SHREE H. N. SHUKLA GROUP OF COLLEGES

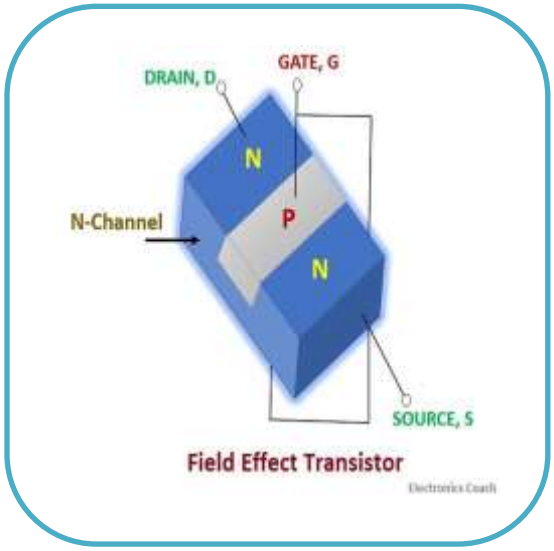
S.Y.B.Sc. SEM – IV

Subject: Physics

Paper- 401

Unit -3

Field Effect Transistor



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- Characteristic of UJT

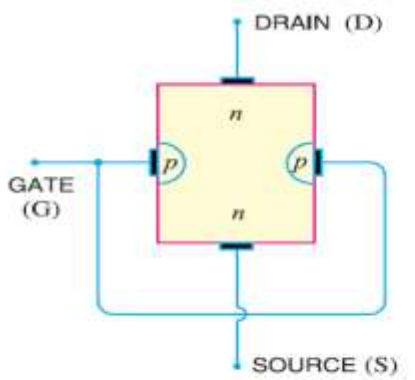
INTRODUCTION:

JUNCTION FIELD EFFECT TRANSISTOR :

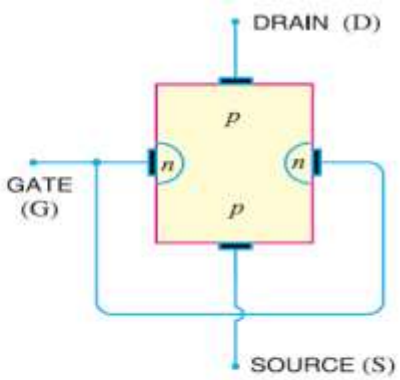
- *" A* **junction field effect transistor** *is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes."*
- The *JFET* was developed about the same time as the transistor but it came into general use only in the late 1960s. In a *JFET*, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The *JFET* has high input impedance and low noise level.

Constructional details :

- A *JFET* consists of a *p*-type or *n*-type silicon bar containing two *pn* junctions at the sides as shown in Fig. The bar forms the conducting channel for the charge carriers. If the bar is of *n*-type, it is called *n-channel JFET* as shown in Fig. (*i*) and if the bar is of *p*-type, it is called a *p-channel JFET* as shown in Fig. (*ii*).
- The two *pn* junctions forming diodes are connected *internally and a common terminal called *gate* is taken out. Other terminals are *source* and *drain* taken out from the bar as shown. Thus a *JFET* has essentially three terminals *viz*. *gate* (*G*), *source* (*S*) and *drain* (*D*).



n-Channel JFET
(*i*)



p-Channel JFET
(*ii*)

- **JFET polarities :** Fig. (*i*) shows *n*-channel *JFET* polarities whereas Fig.(*ii*) shows the *p*-channel *JFET* polarities. Note that in each case, the voltage between the gate and source is such that the gate is reverse biased. This is the normal way of *JFET* connection. The drain and source terminals are interchangeable *i.e.*, either end can be used as source and the other end as drain.

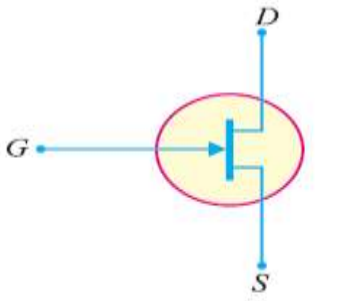
- The following points may be noted :

  (i) The input circuit (*i.e.* gate to source) of a *JFET* is reverse biased. This means that the device has high input impedance.

  (ii) The drain is so biased w.r.t. source that drain current *ID* flows from the source to drain.

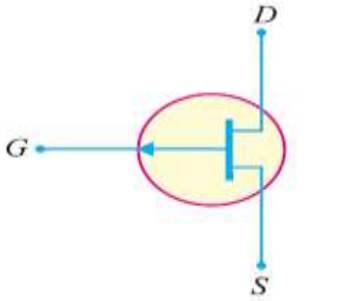
  (iii) In all *JFETs*, source current *IS* is equal to the drain current *i.e.* $I_S = I_D$.

SYMBOL OF JFET :



n-Channel *JFET*

(*i*)



p-Channel *JFET*

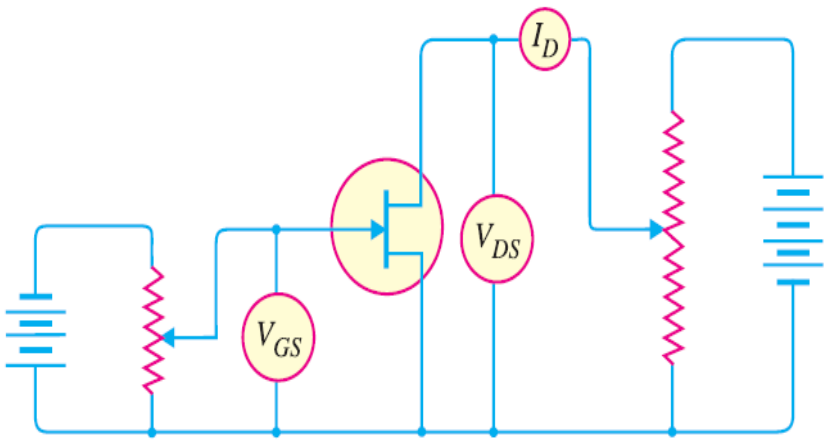
(*ii*)

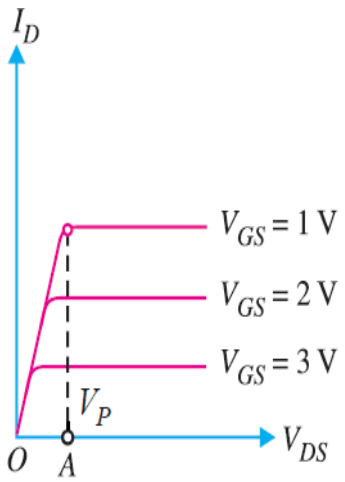
- The vertical line in the symbol may be thought as channel and source (S) and drain (D) connected to this line. If the channel is *n*-type, the arrow on the gate points towards the channel as shown in Fig. (*i*).

- However, for *p*-type channel, the arrow on the gate points from channel to gate [See Fig.(*ii*)].

CHARACTERISTIC OF JFET :

- The curve between drain current (*ID*) and drain-source voltage (*VDS*) of a *JFET* at constant gate source voltage (*VGS*) is known as *output characteristics of JFET*.
- Fig. shows the circuit for determining the output characteristics of *JFET*. Keeping *VGS* fixed at some value, say 1V, the drian source voltage is changed in steps. Corresponding to each value of *VDS*, the drain current *ID* is noted.
- A plot of these values gives the output characteristic of *JFET* at *VGS* = 1V. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. shows a family of output characteristics.





- The following points may be noted from the characteristics :

(i) At first, the drain current *ID* rises rapidly with drain-source voltage *VDS* but then becomes constant. The drain-source voltage above which drain current becomes constant is known as *pinch off voltage*. Thus in Fig. , *OA* is the *pinch off voltage VP*.

(ii) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with *VDS* above pinch off voltage. Consequently, drain current remains constant.

(iii) The characteristics resemble that of a pentode valve.

ADVANTAGES OF JFET :

❁ Some of the advantages of a *JFET* are :

(i) It has a very high input impedance (of the order of 100 MΩ). This permits high degree of isolation between the input and output circuits.

(ii) The operation of a *JFET* depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a *JFET*.

(iii) A *JFET* has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

(iv) A *JFET* has a very high power gain. This eliminates the necessity of using driver stages.

(v) A *JFET* has a smaller size, longer life and high efficiency.

PARAMETERS OF JFET :

❁ A *JFET* has certain parameters which determine its performance in a circuit. The main parameters of a *JFET* are (*i*) a.c. drain resistance (*ii*) transconductance (*iii*) amplification factor.

(*i*) a.c. drain resistance (rd).

Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a *JFET*. It may be defined as follows :

" It is the ratio of change in drain-source voltage (Δ*VDS*) *to the change in drain current* (Δ*ID*) *at constant gate-source voltage". i.e.*

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

Therefore, drain resistance of a *JFET* has a large value, ranging from 10 kΩ to 1 MΩ.

(*ii*) Transconductance (g_{fs}) :

The control that the gate voltage has over the drain current is measured by transconductance *gf s* and is similar to the transconductance *gm* of the tube. It may be defined as follows :

" It is the ratio of change in drain current (Δ*ID*) *to the change in gate-source voltage* (Δ*VGS*) *at constant drain-source voltage". i.e.*

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

The transconductance of a *JFET* is usually expressed either in mA/volt or micromho.

(*iii*) Amplification factor (μ).

" It is the ratio of change in drain-source voltage (ΔVDS) to the change in gate-source voltage (Δ*VGS*) *at constant drain current." i.e.*

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

Amplification factor of a *JFET* indicates how much more control the gate voltage has over drain current than has the drain voltage.

❁ **RELATION AMONG PARAMETER :**

The relationship among *JFET* parameters can be established as under :

$$\text{We know} \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiplying the numerator and denominator on R.H.S. by ΔI_D, we get,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \quad \mu = r_d \times g_{fs}$$

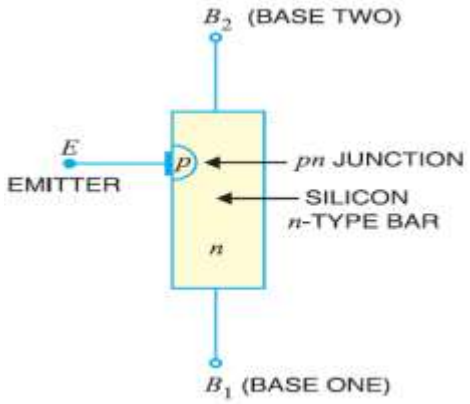
i.e. amplification factor = a.c. drain resistance × transconductance

CONSTRUCTION OF UJT :

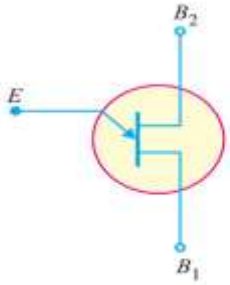
❁ A unijunction transistor (abbreviated as *UJT*) is a three-terminal semiconductor switching device.

❁ This device has a unique characteristic that when it is triggered, the emitter current increases regeneratively until it is limited by emitter power supply.

❁ Due to this characteristic, the unijunction transistor can be employed in a variety of applications *e.g.,* switching, pulse generator, saw-tooth generator etc.



(i)



(ii)

❁ **Construction.** FiG (*i*) shows the basic *structure of a unijunction transistor. It consists of an *n*-type silicon bar with an electrical connection on each end. The leads to these connections are called base leads *base-one* B_1 and *base two* B_2.

❁ Part way along the bar between the two bases, nearer to B_2 than B_1, a *pn* junction is formed between a *p*-type emitter and the bar. The lead to this junctionis called the *emitter lead E*. FiG (*ii*) shows the symbol of unijunction transistor. Note that emitter is shown closer to B_2 than B_1. The following points are worth noting :

(i) Since the device has one *pn* junction and three leads, it is *commonly called a uni junctiontransistor (*uni* means single).

(ii) With only one *pn*-junction, the device is really a form of diode. Because the two base termi-nals are taken from one section of the diode, this device is also called *double-based diode*.

(iii) The emitter is heavily doped having many holes. The *n* region, however, is lightly doped. For this reason, the resistance between the base terminals is very high (5 to 10 k) when emitter leadis open.

CHARACTERISITC OF UJT

Fig. shows the curve between emitter voltage (*VE*) and emitter current (*IE*) of a *UJT* at a given voltage *VBB* between the bases. This is known as the emitter characteristic of *UJT*. The following points may be noted from the characteristics :

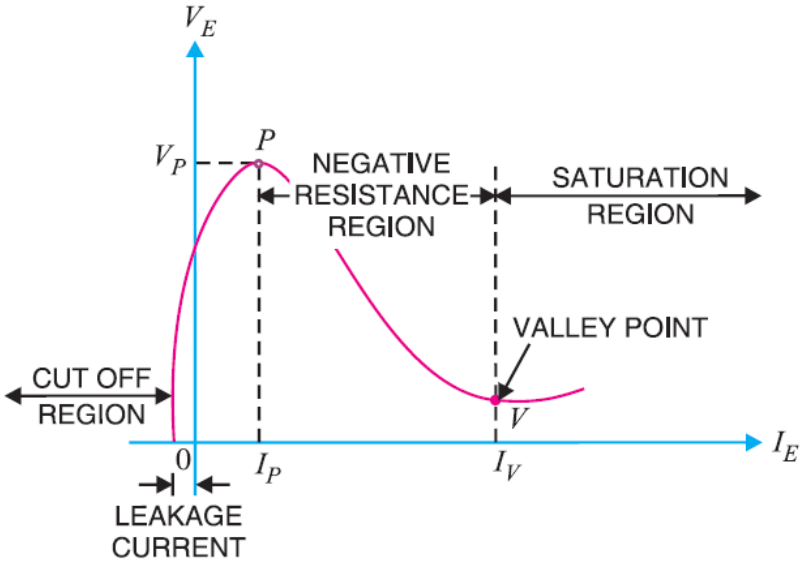
(i) Initially, in the cut-off region, as *VE* increases from zero, slight leakage current flows from terminal *B*2 to the emitter. This current is due to the minority carriers in the reverse biased diode.

(ii) Above a certain value of *VE*, forward *IE* begins to flow, increasing until the peak voltage *VP* and current *IP* are reached at point *P*.

(iii) After the peak point *P*, an attempt to increase *VE* is followed by a sudden increase in emitter current *IE* with a corresponding decrease in *VE*. This is a *negative resistance* portion of the curve because with increase in *IE, VE* decreases.

The device, therefore, has a negative resistance region which is stable enough to be used with a great deal of reliability in many areas *e.g.*, trigger circuits, sawtooth generators, timing circuits .

(iv) The negative portion of the curve lasts until the valley point *V* is reached with valley-point voltage *VV* and valley-point current *IV*. After the valley point, the device is driven to saturation.



ADVANTAGE OF UJT :

- The *UJT* was introduced in 1948 but did not become commercially available until 1952. Since then, the device has achieved great popularity due to the following reasons :

(*i*) It is a low cost device.

(*ii*) It has excellent characteristics.

(*iii*) It is a low-power absorbing device under normal operating conditions.

- Due to above reasons, this device is being used in a variety of applications. A few include oscillators, trigger circuits, saw-tooth generators, bistable network etc.