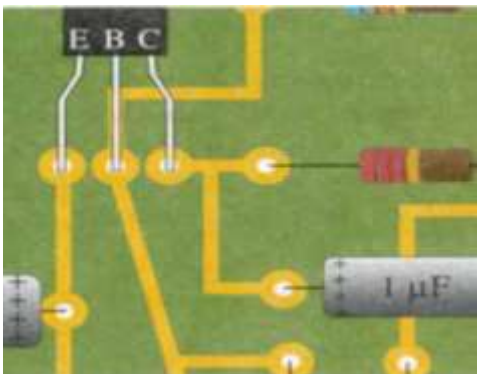
S.Y.B.Sc. SEM – III

Subject: Physics

Paper- 301

Unit -5

TRANSISTOR BIASING & STABILISATION OF OPERATING POINT



- Introduction
- Review of transistor connection
- Load line analysis
- Operating point
- Transistor biasing
- stabilization
- Method of transistor biasing
- Base resister method
- Voltage divider bias method

❖ TITLE JUSTIFICATION :

The title justified as that the transistor is a semiconductor device and its use to regulate the supply current or voltage. It can be used as a **switch** in electrical circuits and also use as an **amplifier** also in our daily life electronic appliances. Now a days, They are used in almost every electronics devices , so for their better use we have improve their biasing method and stability of instrument.

❖ THEME :

In this chapter in electronics, **biasing** is the setting of initial operating conditions (current and voltage) of an active device in an amplifier. Many electronic devices, such as diodes**, & transistors.** For their better use we have to improve transistor biasing method. Due to biasing we got best operating point of device and electronic device will be more stable. In this chapter we study different kind of biasing method.

❖ INTRODUCTION :

A transistor can work as an amplifier in forward bias and reverse bias. One important requirement during amplification is that only magnitude of the signal is known as faithful amplification. In this chapter we will discuss about operating point, stabilization, and various method of transistor biasing.

❖ Review of Transistor Connection:

- There are three leads in a transistor *viz*., emitter, base and collector terminals. However, when a Transistor is to be connected in a circuit; we require four terminals; two for the input and two for the output. This difficulty is overcome by making one terminal of the transistor common to both input and output terminals.
- The input is fed between this common terminal and one of the other two terminals. The output is obtained between the common terminal and the remaining terminal. Accordingly; a transistor can be connected in a circuit in the following three ways :
  - ***(i)*** **common base connection**
  - ***(ii)*** **common emitter connection**
  - ***(iii)*** **common collector connection**
- Each circuit connection has specific advantages and disadvantages. It may be noted here that regardless of circuit connection, the emitter is always biased in the forward direction, while the collector always has a reverse bias.

SRNO	QUESTION	ANSWER
1	A transistor work as a amplifier of the E-B junction is _____.	Forward bias
2	A transistor work as a amplifier of the C-B junction is _____.	Reverse bias
3	How many connecting leads in a transistor namely?	Base, Collector, Emitter
4	Mention that how transistor can be connected in a circuit namely?	Common base, Common collector, Common emitter

❖ LOAD LINE ANALYSIS:

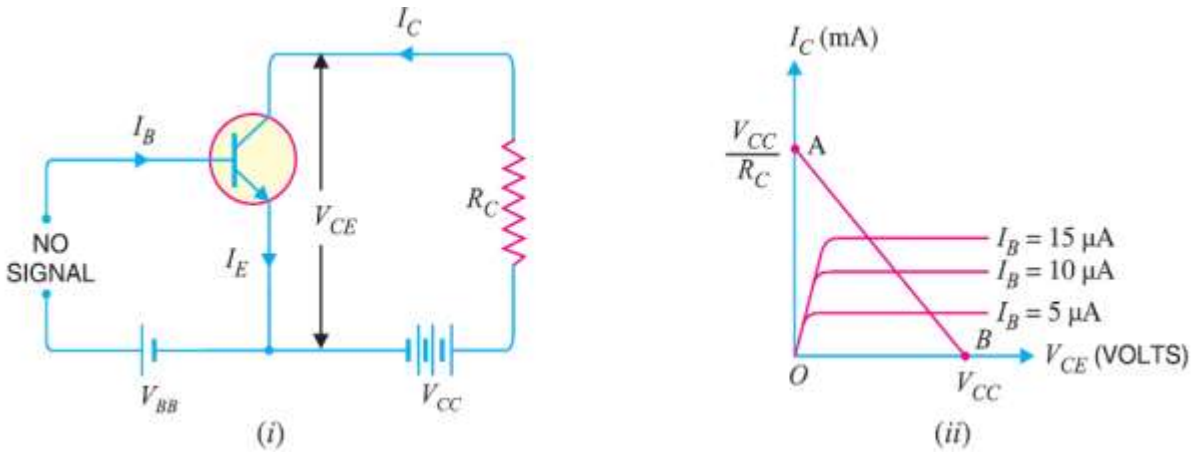
In the transistor circuit analysis, it is generally required to determine the collector current for various collector-emitter voltages. One of the methods can be used to plot the output characteristics and determine the collector current at any desired collector-emitter voltage. However, a more convenient method, known as *load line method* can be used to solve such problems.

- D.C. Load Line:

  Consider a common emitter *npn* transistor circuit shown in Fig. (*i*) Where no signal is applied. Therefore, D.C. conditions prevail in the circuit. The output characteristics of this circuit are shown in Fig. (*ii*).

The value of collector-emitter voltage V_{CE} at any time is given by;

$$V_{CE} = V_{CC} - I_C R_C \ldots (i)$$



As V_{CC} and R_C are fixed values, therefore, it is a first degree equation and can be represented by a straight line on the output characteristics. This is known as *d.c. load line* and determines the locus of V_{CE} - I_C points for any given value of R_C. To add load line, we need two end points of the straight-line.

1. When the collector current $I_C = 0$, then collector-emitter voltage is maximum and is equal to V_{CC} *i.e.* Max. $V_{CE} = V_{CC} - I_C R_C = V_{CC}$ (ä $I_C = 0$) this gives the first point B ($OB = V_{CC}$) on the collector-emitter voltage axis as shown in Fig. (*ii*).

2. When collector-emitter voltage VCE = 0, the collector current is maximum and is equal to V_{CC}/R_C *i.e.* $V_{CE} = V_{CC} - I_C R_C$ or $0 = V_{CC} - I_C R_C$. Max. $I_C = V_{CC}/R_C$. This gives the second point A ($OA = V_{CC}/R_C$) on the collector current axis as shown in Fig. (*ii*). By joining these two points, d.c. *load line AB Is constructed.

SR NO	QUESTION	ANSWER
1	Transistor biasing represents..... Conditions.	d.c.
2	The collector emitter voltage is maximum or equal to Vcc then value of Ic = _____.	Ic = 0
3	The collector emitter voltage is zero or then value of Ic = _____.	Vcc / Rc

1. OPERATING POINT:

"The zero signal values of I_C and V_{CE} are known as the **operating point**."

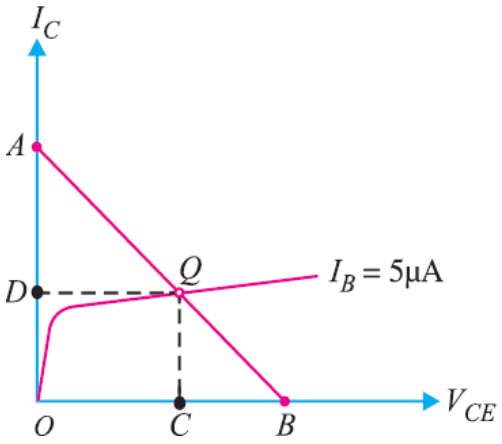


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Fig 3

- It is called operating point because the variations of I_C and V_{CE} take place about this point when signal is applied. It is also called quiescent (silent) point or *Q-point* because it is the point on $I_C - V_{CE}$ characteristic when the transistor is silent *i.e.* in the absence of the signal.

- Suppose in the absence of signal, the base current is 5 μA. Then I_C and V_{CE} conditions in the circuit must be represented by some point on I_B = 5 μA characteristic. But I_C and V_{CE} conditions in the circuit should also be represented by some point on the D.C. load line *AB*.
- The point *Q* where the load line and the characteristic intersect is the only point which satisfies both these conditions. Therefore, the point *Q* describes the actual state of affairs in the circuit in the zero signal conditions and is called the operating point.
- for *IB* = 5 μA, the zero signal values are : V_{CE} = *OC* volts I_C = *OD* mA It follows, therefore, that the zero signal values of I_C and V_{CE} (*i.e.* operating point) are determined by the point where d.c. load line intersects the proper base current curve.

SR NO	QUESTION	ANSWER
1	The zero signal values of I_C and V_{CE} are known as the _____.	Operating point
2	Operating point represents _____.	Zero signal values of IC and VCE
3	The point of intersection of d.c. and a.c. load lines represents _____.	Operating point
4	The operating point is also called the _____.	Quiescent point

2. Performance of Transistor Amplifier :

The performance of a transistor amplifier depends upon input resistance, output resistance, effective collector load, current gain, voltage gain and power gain.

(i) Input resistance. *It is the ratio of small change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage i.e.*

$$\text{Input resistance, } R_i = \frac{\Delta V_{BE}}{\Delta I_B}$$

***ii*) Output resistance.** *It is the ratio of change in collector emitter voltage* (ΔVCE) *to the resulting change in collector current* (ΔIC) *at constant base current.*

$$\text{Output resistance, } R_O = \frac{\Delta V_{CE}}{\Delta I_C}$$

(iii) Effective collector load. *It is the total load as seen by the a.c. collector current.*

(iv) Current gain. *It is the ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B) i.e.*

$$\text{Current gain, } \beta = \frac{\Delta I_C}{\Delta I_B}$$

(v) Voltage gain. *It is the ratio of change in output voltage (ΔV_{CE}) to the change in input voltage (ΔV_{BE}) i.e.*

$$\text{Voltage gain, } A_v = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

$$= \frac{\text{Change in output current} \times \text{effective load}}{\text{Change in input current} \times \text{input resistance}}$$

$$= \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i} = \frac{\Delta I_C}{\Delta I_B} \times \frac{R_{AC}}{R_i} = \beta \times \frac{R_{AC}}{R_i}$$

(vi) Power gain. *It is the ratio of output signal power to the input signal power i.e.*

$$\text{Power gain, } A_p = \frac{(\Delta I_C)^2 \times R_{AC}}{(\Delta I_B)^2 \times R_i} = \left(\frac{\Delta I_C}{\Delta I_B}\right) \times \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i}$$

$$= \text{Current gain} \times \text{Voltage gain}$$

Sr.no	QUESTION	ANSWER
1	It is the ratio of small change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage is known as _____.	Input resistance.
2	It is the ratio of change in collector emitter voltage (ΔV_{CE}) to the resulting change in collector current (ΔI_C) at constant base current is known as_____.	Output resistance.
3	It is the ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B) is known as _____.	Current gain
4	It is the ratio of change in output voltage (ΔV_{CE}) to the change in input voltage (ΔV_{BE}) is known as _____.	Voltage gain
5	It is the ratio of output signal power to the input signal power is known as _____.	Power gain

3. Cut off and Saturation Points :

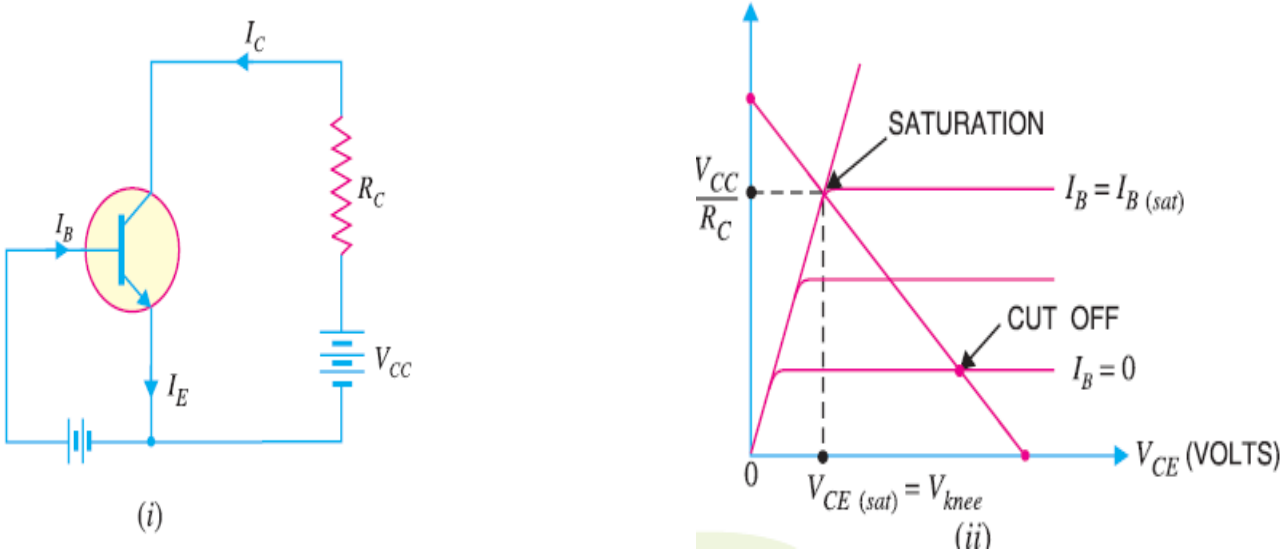


Fig-4

(*i*) Cut off :

The point where the load line intersects the $I_B = 0$ curve is known as *cut off*. At this point, $I_B = 0$ and only small collector current (*i.e.* collector leakage current I_{CEO}) exists. At cut off, the base-emitter junction no longer remains forward biased and normal transistor action is lost. The collector-emitter voltage is nearly equal to V_{CC}.

$$V_{CE}\ (cut\ off) = V_{CC}$$

(*ii*) Saturation:

The point where the load line intersects the $I_B = I_B\ (sat)$ curve is called *saturation*. At this point, the base current is maximum and so is the collector current. At saturation, collector base junction no longer remains reverse biased and normal transistor action is lost.

$$I_{C\ (sat)} \simeq \frac{V_{CC}}{R_C};\quad V_{CE} = V_{CE(sat)} = V_{knee}$$

If base current is greater than $I_B\ (sat)$, then collector current cannot increase because collector-base junction is no longer reverse-biased.

(iii) Active region:

The region between cut off and saturation is known as *active region*. In the active region, collector-base junction remains reverse biased while base-emitter junction remains forward biased. Consequently, the transistor will function normally in this region.

SR NO	QUESTION	ANSWER
1	In CUT OFF region the value of I_C = _____.	0
2	In SATURATION region the value of I_C = _____.	I_E
3	In ACTIVE region the value of I_C = _____.	**β** I_B
4	In _____ region emitter diode and collector diode are OFF.	Cut off
5	In _____ region emitter diode is ON & collector diode is OFF.	Active
6	In _____ region emitter diode and collector diode are On.	Saturation

4. Power Rating of Transistor :

"The maximum power that a transistor can handle without destruction is known as **power rating** of the transistor."

- When a transistor is in operation, almost all the power is dissipated at the reverse biased *collector-base junction. The power rating (or maximum power dissipation) is given by:

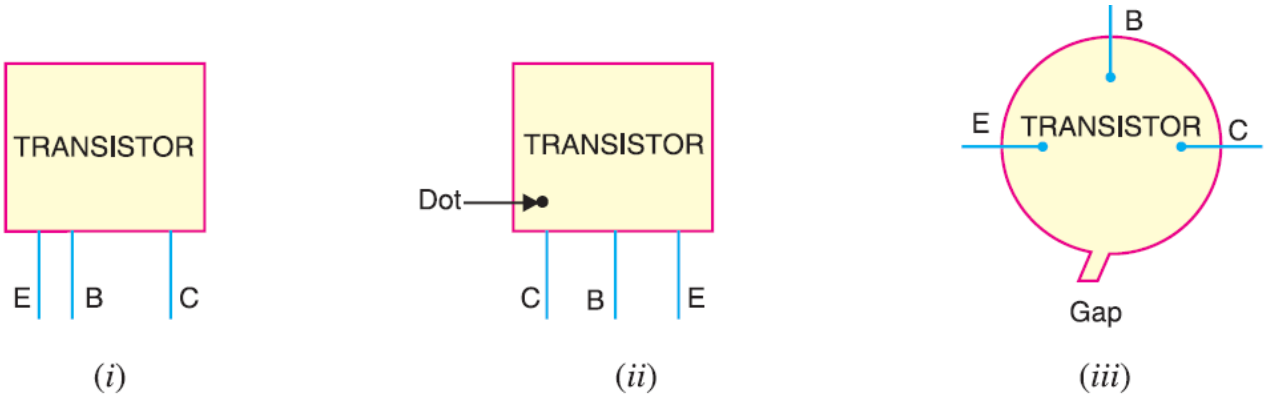
$$P_{D\ (max)} = \text{Collector current} \times \text{Collector-base voltage}$$
$$= I_C \times V_{CB}$$
$$P_{D\ (max)} = I_C \times V_{CE}$$

$[\because V_{CE} = V_{CB} + V_{BE}.$ Since V_{BE} is very small, $V_{CB} \simeq V_{CE}]$

- While connecting transistor in a circuit, it should be ensured that its power rating is not exceeded Otherwise the transistor may be destroyed due to excessive heat.

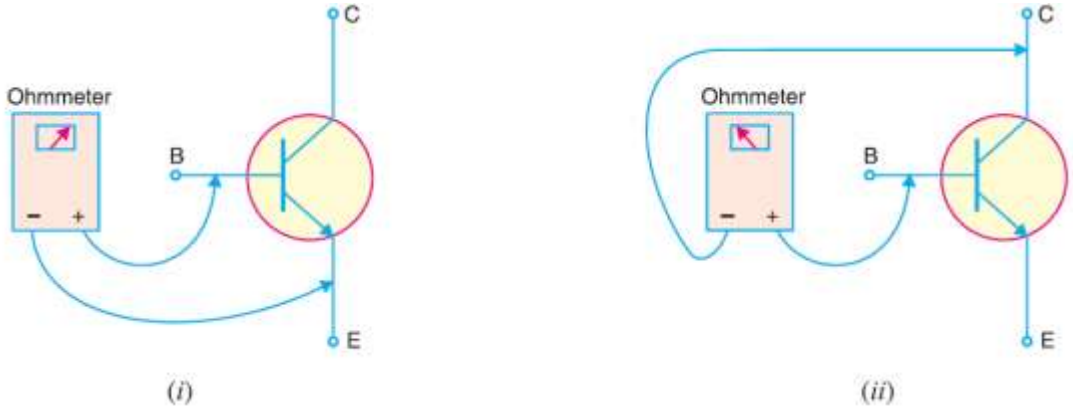
5. Transistor Lead Identification :

- There are three leads in a transistor *viz*. collector, emitter and base.
- When the leads of a transistor are in the same plane and unevenly spaced [See Fig. (*i*)], they are identified by the positions and spacing of leads. The central lead is the base lead. The collector lead is identified by the larger spacing existing between it and the base lead. The remaining lead is the emitter.
- When the leads of a transistor are in the same plane but evenly spaced [See Fig. (*ii*)], the central lead is the base, the lead identified by dot is the collector and the remaining lead is the emitter.
- When the leads of a transistor are spaced around the circumference of a circle [See Fig. (*iii*)], the three leads are generally in E-B-C order clockwise from a gap.



6. Transistor Testing :

- Below Fig. shows the process of testing an *npn* transistor with an ohmmeter.



(i) The forward biased base-emitter junction (biased by internal supply) should read a low resistance, typically 100 Ω to 1 kΩ as shown in Fig. (*i*). If that is so, the transistor is good. However, if it fails this check, the transistor is faulty and it must be replaced.

(ii) The reverse biased collector-base junction (again reverse biased by internal supply) should be checked as shown in Fig. (*ii*). If the reading of the ohmmeter is 100 kΩ or higher, the transistor is good. If the ohmmeter registers a small resistance, the transistor is faulty and requires replacement.

SR NO	QUESTION	ANSWER
1	A capacity transistor to handle a power without destruction is known as _____.	Power rating
2	How many leads namely in transistor?	3leads , Collector, Emitter, Base
3	The leads of a transistor are in the same plane and unevenly spaced the central lead is the_____ lead.	Base
4	The leads of a transistor are in the same plane but evenly spaced & identified by dot is the _____.	Collector
5	The transistor leads are on a circle they are arranged in E-B-C order in _____ direction.	Clockwise
6	The forward biased base-emitter junction (biased by internal supply) should read _____ a resistance.	Low
7	The reverse biased collector-base junction (reverse biased by internal supply) should be read_____ a Resistance.	Higher

7. Faithful Amplification :

"The process of raising the strength of a weak signal without any change in its general shape is known as **faithful amplification."**

- The theory of transistor reveals that it will function properly if its input circuit (*i.e.* base-emitter junction) remains forward biased and output circuit (*i.e.* collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification.
- To ensure this, the following basic conditions must be satisfied:

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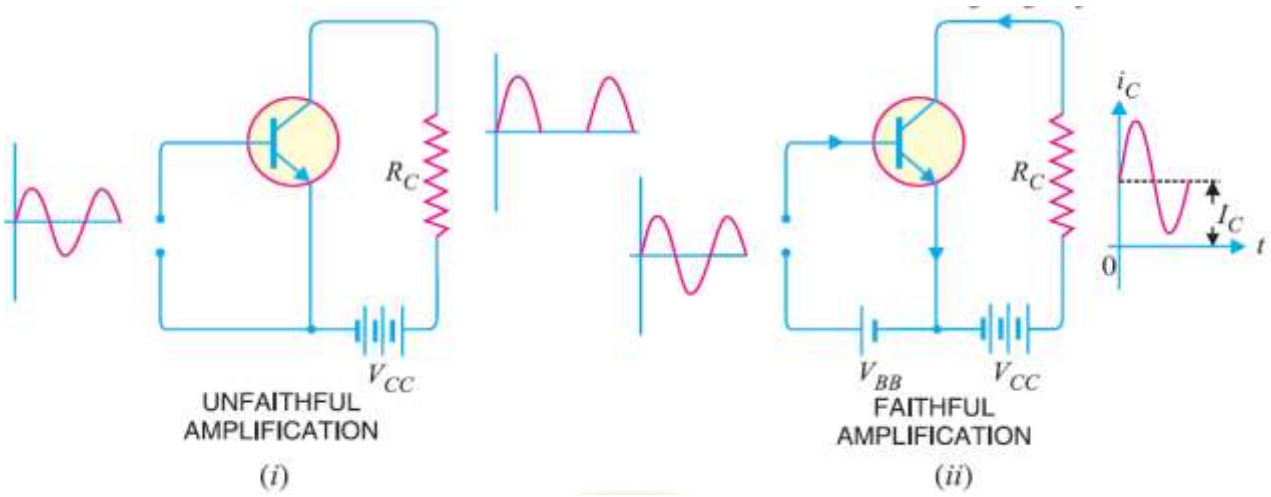
(*i*) Proper zero signal collector current

(*ii*) Minimum proper base-emitter voltage (V_{BE}) at any instant

(iii) Minimum proper collector-emitter voltage (V_{CE}) at any instant.

1. Proper zero signal collector current :



- Consider an *NPN* transistor circuit shown in Fig (*i*). During the positive half-cycle of the signal, base is positive w.r.t. emitter and hence base emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit.
- The result is that positive half-cycle of the signal is amplified in the collector. However, during the negative half-cycle of the signal, base-emitter junction is reverse biased and hence no current flows in the circuit.
- The result is that there is no output due to the negative half cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is unfaithful amplification.
- Now, introduce a battery source *VBB* in the base circuit as shown in Fig. (*ii*). The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} . This is known as *zero signal collector current* I_C.

- During the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases. However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases.
- In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows, therefore, that for faithful amplification, proper zero signal collector current must flow. "*The value of zero signal collector current should be at least equal to the maximum collector current due to signal alone".*

2. Proper minimum base-emitter voltage:

- In order to achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below 0.5V for germanium transistors and 0.7V for *Si* transistors at any instant.

- The base current is very small until the *input voltage overcomes the potential barrier at the base-emitter junction. The value of this potential barrier is 0.5V for Ge transistors and 0.7V for *Si* transistors as shown in above fig. Once the potential barrier is overcome, the base current and hence collector current increases sharply.
- Therefore, if base-emitter voltage V_{BE} falls below these values during any part of the signal, that part will be amplified to lesser extent due to small collector current. This will result in unfaithful amplification.

3. Proper minimum V_{CE} at any instant :

For faithful amplification, the collector-emitter voltage V_{CE} should not fall below 0.5V for Ge transistors and 1V for silicon transistors. This is called" *knee voltage".*

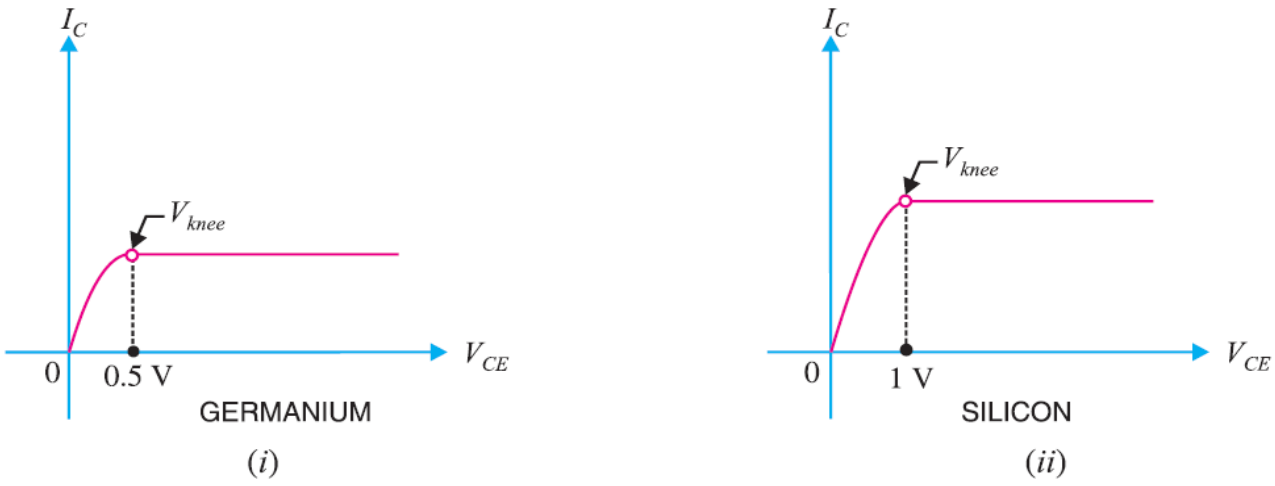


Fig -

- When V_{CE} is too low the collector base junction is not properly reverse biased. Therefore, the collector cannot attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base.
- This decreases the collector current while base current increases. Hence, value of β falls. Therefore, if *VCE* is allowed to fall below *Vknee* during any part of the signal, that part will be less amplified due to reduced β.
- This will result in unfaithful amplification. However, when V_{CE} is greater than *Vknee*, the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

SRNO	QUESTION	ANSWER
1.	The process of raising the strength of a weak signal without any change in its general shape is known as _____.	Faithful amplification.
2.	Write any one condition for faithful amplification.	Proper zero signal collector current
3.	When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} is known as_____.	zero signal collector current
4.	To achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below _____ for germanium transistors.	0.5V
5.	To achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below _____ for *Si* transistors.	0.7 V
6.	For faithful amplification, the collector-emitter voltage V_{CE} should not fall below 0.5V for Ge transistors and 1V for silicon transistors it is called _____.	Knee voltage
7.	If the temperature increases, the value of V_{BE} _____.	is decreased

❖ Transistor Biasing :

- A transistor amplifier must satisfy three conditions for faithful amplification. If It is the fulfillment of these conditions which is known as transistor biasing.

"The proper flow of zero signal collectors current and the maintenance of proper collector-emitter voltage during the passage of signal is known as **transistor biasing**.**"**

- The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal.
- This can be achieved with a bias battery or associating a circuit with a transistor. The latter method is more efficient and is frequently employed. The circuit which provides transistor biasing is known as "*biasing circuit*."
-

❖ Inherent Variations of Transistor Parameters :

- In practice, the transistor parameters such as β, V_{BE} are not the same for every transistor even of the same type. To give an example, BC147 is a silicon *npn* transistor with β varying from 100 to 600 *i.e.* β for one transistor may be 100 and for the other it may be 600, although both of them are *BC*147. This large variation in parameters is a characteristic of transistors.
- The major reason for these variations is that transistor is a new device and manufacturing techniques have not too much advanced. For instance, it has not been possible to control the base width and it may vary, although slightly, from one transistor to the other even of the same type. Such small variations result in large change in transistor parameters such as β, V_{BE} etc.

- The inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification. It is, therefore, very important that biasing network be so designed that it should be able to work with all transistors of one type whatever may be the spread in β or V_{BE}. In other words, the operating point should be independent of transistor parameters variations.

SR NO	QUESTION	ANSWER
1	In CUT OFF region the value of I_C = _____.	0
2	In SATURATION region the value of I_C = _____.	I_E
3	In ACTIVE region the value of I_C = _____.	**β** I_B

❖ Stabilization :

- The collector current in a transistor changes rapidly when

  (*i*) The temperature changes,

  (*ii*) The transistor is replaced by another of the same type.

- This is due to the inherent variations of transistor parameters. When the temperature changes or the transistor is replaced, the operating point (*i.e*. zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. This necessitates making the operating point independent of these variations. This is known as stabilization.

"The process of making operating point independent of temperature changes or variations in transistor parameters is known as Stabilization."

- Once stabilization is done, the zero signal I_C and V_{CE} become independent of temperature variations or replacement of transistor *i.e.* the operating point is fixed. A good biasing circuit always ensures the stabilization of operating point.

❖ Need for stabilization:

Stabilization of the operating point is necessary due to the following reasons:

(*i*) Temperature dependence of *IC*

(*ii*) Individual variations

(*iii*) Thermal runaway

(*i*) Temperature dependence of I_C :

The collector current I_C for CE circuit is given by:

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 10°C doubles the collector leakage current which may be as high as 0.2 mA for low powered germanium transistors.

As biasing conditions in such transistors are generally so set that zero signal I_C = 1mA, therefore, the change in I_C due to temperature variations cannot be tolerated. This necessitates stabilizing the operating point *i.e*. to hold I_C constant inspite of temperature variations.

(*ii*) Individual variations:

The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates stabilizing the operating point *i.e*. to hold I_C constant irrespective of individual variations in transistor parameters.

(*iii*) Thermal run away :

The collector current for a *CE* configuration is given by : $I_C = \beta I_B + (\beta + 1) I_{CBO}$ ...(*i*)

The collector leakage current I_{CBO} is strongly dependent on temperature. The flow of collector current produces heat within the transistor. This raises the transistor temperature and if no stabilisation is done, the collector leakage current I_{CBO} also increases. It is clear from exp. (*i*) that if I_{CBO} increases, the collector current *IC* increases by (β + 1) I_{CBO}.

The increased I_C will raise the temperature of the transistor, which in turn will cause I_{CBO} to increase. This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out.

"The self-destruction of an unstabilised transistor is known as thermal runaway."

In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is stabilized *i.e.* I_C is kept constant.

In practice, this is done by causing I_B to decrease automatically with temperature increase by circuit modification. Then decrease in βI_B will compensate for the increase in $(\beta + 1) I_{CBO}$, keeping I_C nearly constant. In fact, this is what is always aimed at while building and designing a biasing circuit.

SR NO	QUESTION	ANSWER
1.	The collector current in a transistor changes rapidly when _____ changes.	Temperature
2.	The process of making operating point independent of temperature changes or variations in transistor parameters is known as _____.	Stabilization.
3.	State any one reason for stabilization of the operating point is necessary:	Temperature dependence of *IC*
4.	The self-destruction of an unstabilised transistor is known as _____	thermal runaway
5.	In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is _____.	Stabilised
6.	Thermal runaway occurs when _____.	transistor is not biased

❖ Essentials of a Transistor Biasing Circuit :

It has already been discussed that transistor biasing is required for faithful amplification. The biasing network associated with the transistor should meet the following requirements:

(*i*) It should ensure proper zero signal collector current.

(*ii*) It should ensure that V_{CE} does not fall below 0.5 V for *Ge* transistors and 1 V for silicon transistors at any instant.

(*iii*) It should ensure the stabilisation of operating point.

❖ Stability Factor :

- It is desirable and necessary to keep I_C constant in the face of variations of I_{CBO} (sometimes represented as I_{CO}). The extent to which a biasing circuit is successful in achieving this goal is measured by stability factor *S*. It is defined as under:

"The rate of change of collector current I_C w.r.t. the collector leakage current *I_{CO} at constant β and I_B is called stability factor".

$$\text{Stability factor, } S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

- The stability factor indicates the change in collector current I_C due to the change in collector leakage current I_{CO}. Thus a stability factor 50 of a circuit means that *IC* changes 50 times as much as any change in *ICO*. In order to achieve greater thermal stability, it is desirable to have as low stability factor as possible.
- The ideal value of *S* is 1 but it is never possible to achieve it in practice. Experience shows that values of S exceeding 25 result in unsatisfactory performance.

The general expression of stability factor for a C.E. configuration can be obtained as under:

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

** Differentiating above expression *w.r.t.* I_C, we get,

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

or
$$1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S} \qquad \left[\because \frac{dI_{CO}}{dI_C} = \frac{1}{S}\right]$$

or
$$S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

SR NO	QUESTION	ANSWER
1.	For essential of biasing circuit It should ensure that V_{CE} does not fall below _____ for *Ge* transistors and _____ for Si transistors at any instant.	0.5 V , 1 V
2.	For essential of biasing circuit It should ensure proper zero signal _____ current	Collector
3.	The rate of change of collector current I_C w.r.t. the collector leakage current *I_{CO} at constant β and I_B is called _____.	Stability factor
4.	An ideal value of stability factor is _____.	1
5.	Expression of stability factor S = _____.	$S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$

❖ Methods of Transistor Biasing :

The following are the most commonly used methods of obtaining transistor biasing from one source of supply (*i.e.* V_{CC}) :

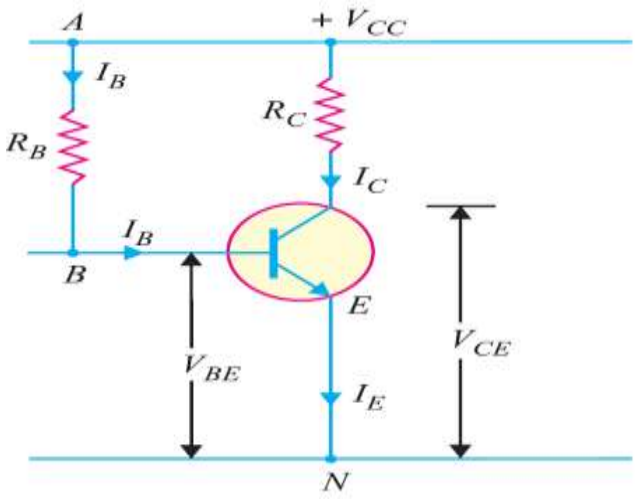
(i) Base resistor method

(ii) Emitter bias method

(iii) Biasing with collector-feedback resistor

(iv) Voltage-divider bias.

❖ Base Resistor Method :



- In this method, a high resistance R_B (several hundred kΩ) is connected between the base and +ve end of supply for *npn* transistor (See above Fig.) and between base and negative end of supply for *pnp* transistor. Here, the required zero signal base current is provided by V_{CC} and it flows through R_B.
- It is because now base is positive *w.r.t.* emitter *i.e.* base-emitter junction is forward biased. The required value of zero signal base current I_B (and hence $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor R_B.

❖ Circuit analysis:

It is required to find the value of *RB* so that required collector current flows in the zero signal conditions. Let *IC* be the required zero signal collector current.

$$\therefore \quad I_B = \frac{I_C}{\beta}$$

Considering the closed circuit *ABENA* and applying Kirchhoff's voltage law, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

or $$I_B R_B = V_{CC} - V_{BE}$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} \qquad \ldots (i)$$

As V_{CC} and I_B are known and V_{BE} can be seen from the transistor manual, therefore, value of R_B can be readily found from exp. (*i*).

Since V_{BE} is generally quite small as compared to V_{CC}, the former can be neglected with little error. It then follows from exp. (*i*) that :

$$R_B = \frac{V_{CC}}{I_B}$$

It may be noted that V_{CC} is a fixed known quantity and I_B is chosen at some suitable value. Hence, R_B can always be found directly, and for this reason, this method is sometimes called *fixed-bias method.*

❖ Stability factor:

$$\text{Stability factor,} \quad S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

In fixed-bias method of biasing, I_B is independent of I_C so that $dI_B/dI_C = 0$. Putting the value of $dI_B / dI_C = 0$ in the above expression, we have,

$$\text{Stability factor,} \quad S = \beta + 1$$

Thus the stability factor in a fixed bias is $(\beta + 1)$. This means that I_C changes $(\beta + 1)$ times as much as any change in I_{CO}. For instance, if $\beta = 100$, then $S = 101$ which means that I_C increases 101 times faster than I_{CO}. Due to the large value of S in a fixed bias, it has poor thermal stability.

❖ Advantages :

(*i*) This biasing circuit is very simple as only one resistance R_B is required.

(*ii*) Biasing conditions can easily be set and the calculations are simple.

(*iii*) There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

❖ Disadvantages :

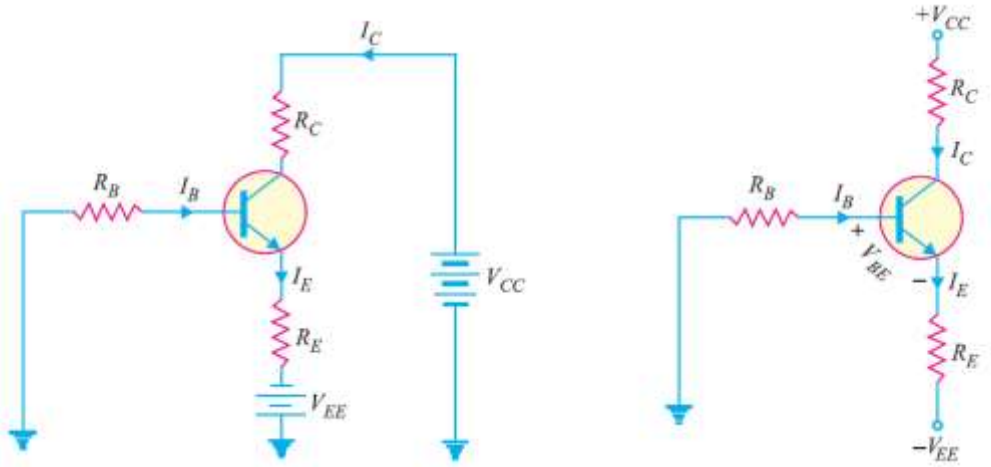
(*i*) This method provides poor stabilization. It is because there is no means to stop a self increase in collector current due to temperature rise and individual variations. For example, if β increases due to transistor replacement, then I_C also increases by the same factor as I_B is constant.

(*ii*) The stability factor is very high. Therefore, there are strong chances of thermal runaway. Due to these disadvantages, this method of biasing is rarely employed.

SR NO	QUESTION	ANSWER
1.	Write any one method for transistor biasing?	Base resistor method
2.	The base resistor method is generally used in.....	switching circuits
3.	The value of stability factor for a base-resistor bias is.....	(β + 1)
4.	In a base resistor method, if the value of β changes by 50, then collector current will change by a factor of.....	50
5.	For base resistor method the value of stability factor is very _____.	High
6.	The main disadvantage of base resistor method is _____.	Thermal runway
7.	Base resistor methods give _____ stabilization.	Poor

❖ Emitter Bias Circuit :

Below Fig. shows the emitter bias circuit. This circuit differs from base-bias circuit in two important respects. First, it uses two separate d.c. voltage sources; one positive (+ V_{CC}) and the other negative (– V_{EE}). Normally, the two supply voltages will be equal. For example, if V_{CC} = + 20V (d.c.), then V_{EE} = – 20V (d.c.). Secondly, there is a resistor R_E in the emitter circuit.



We shall first redraw the circuit in above Fig. as it usually appears on schematic diagrams. This Means deleting the battery symbols as shown in Fig. All the information is still (See Fig.) on the diagram except that it is in condensed form. That is a negative supply voltage – V_{EE} is applied to the bottom of R_E and a positive voltage of + V_{CC} to the top of R_C.

❖ Circuit Analysis of Emitter Bias :

Fig. shows the emitter bias circuit. We shall find the Q-point values (*i.e.* D.C. I_C and D.C. V_{CE}) for this circuit.

(*i*) Collector current (I_C): Applying Kirchhoff's voltage law to the base-emitter circuit in Fig, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$V_{EE} = I_B R_B + V_{BE} + I_E R_E$$

Now $I_C \simeq I_E$ and $I_C = \beta I_B \quad \therefore I_B \simeq \frac{I_E}{\beta}$

Putting $I_B = I_E/\beta$ in the above equation, we have,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or $$V_{EE} - V_{BE} = I_E (R_B/\beta + R_E)$$

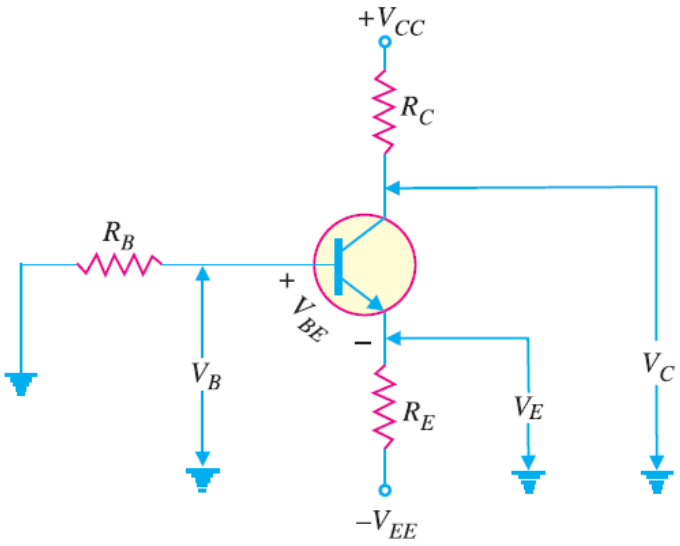
$$\therefore \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Since $I_C \simeq I_E$, we have,

$$I_C = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

(*ii*) Collector-emitter voltage (V_{CE}):

Below fig. shows the various voltages of the emitter bias circuit w.r.t. ground.



Emitter voltage w.r.t. ground is

$$V_E = -V_{EE} + I_E R_E$$

Base voltage w.r.t. ground is

$$V_B = V_E + V_{BE}$$

Collector voltage w.r.t. ground is

$$V_C = V_{CC} - I_C R_C$$

Subtracting V_E from V_C and using the approximation $I_C \simeq I_E$, we have,

$$V_C - V_E = (V_{CC} - I_C R_C) - (-V_{EE} + I_C R_E) \qquad (\because I_E \simeq I_C)$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

Alternatively: Applying Kirchhoff's voltage law to the collector side of the emitter bias circuit in Fig. (Refer back), we have,

$$V_{CC} - I_C R_C - V_{CE} - I_C^* R_E + V_{EE} = 0$$
$$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

Stability of Emitter bias: The expression for collector current I_C for the emitter bias circuit is given by

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B / \beta}$$

It is clear that I_C is dependent on V_{BE} and β, both of which change with temperature.

If $R_E >> R_B/\beta$, then expression for I_C becomes :

$$I_C = \frac{V_{EE} - V_{BE}}{R_E}$$

This condition makes $I_C (\simeq I_E)$ independent of β.

If $V_{EE} >> V_{BE}$, then I_C becomes :

$$I_C (\simeq I_E) = \frac{V_{EE}}{R_E}$$

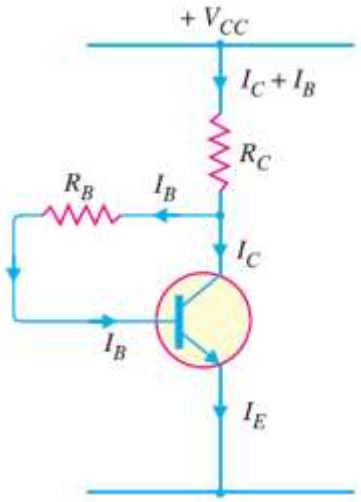
This condition makes $I_C (\simeq I_E)$ independent of V_{BE}.

If $I_C (\simeq I_E)$ is independent of β and V_{BE}, the Q-point is not affected appreciably by the variations in these parameters. Thus emitter bias can provide stable Q-point if properly designed.

SR NO	QUESTION	ANSWER
1.	In emitter bias circuit there are _____ separate d.c. voltage sources, one is _____ and the other is _____.	Two , Positive , Negative
2.	The purpose of resistance in the emitter circuit of a transistor amplifier is to.....	Limit the change in emitter current
3.	In emitter bias circuit Q point value depends on _____ and _____.	Collector current (I_C), Collector-emitter voltage (V_{CE})
4.	_____ biasing provides stable Q- point.	Emitter bias

❖ Biasing with Collector Feedback Resistor :

- In this method, one end of R_B is connected to the base and the other end to the collector as shown in below Fig. Here, the required zero signal base current is determined *not* by V_{CC} but by the collector base voltage V_{CB}. It is clear that V_{CB} forward biases the base-emitter junction and hence base current I_B flows through R_B. This causes the zero signal collector current to flow in the circuit.



❖ Circuit analysis:

The required value of R_B needed to give the zero signals current I_C can be determined as follows.

Referring to above Fig.

$$V_{CC} = I_C R_C + I_B R_B + V_{BE}$$

or
$$R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B}$$

$$= \frac{V_{CC} - V_{BE} - \beta I_B R_C}{I_B} \quad (\because I_C = \beta I_B)$$

Alternatively, $V_{CE} = V_{BE} + V_{CB}$

or $V_{CB} = V_{CE} - V_{BE}$

$$\therefore \quad R_B = \frac{V_{CB}}{I_B} = \frac{V_{CE} - V_{BE}}{I_B}; \quad \text{where} \quad I_B = \frac{I_C}{\beta}$$

- It can be shown mathematically that stability factor S for this method of biasing is less than $(\beta + 1)$ *i.e.* Stability factor, $S < (\beta + 1)$. Therefore, this method provides better thermal stability than the fixed bias.

❖ Advantages :

(*i*) It is a simple method as it requires only one resistance R_B.

(*ii*) This circuit provides some stabilization of the operating point as discussed below :

$$V_{CE} = V_{BE} + V_{CB}$$

Suppose the temperature increases. This will increase collector leakage current and hence the total collector current. But as soon as collector current increases, V_{CE} decreases due to greater drop across R_C. The result is that V_{CB} decreases *i.e.* lesser voltage is available across R_B. Hence the base current I_B decreases. The smaller I_B tends to decrease the collector current to original value.

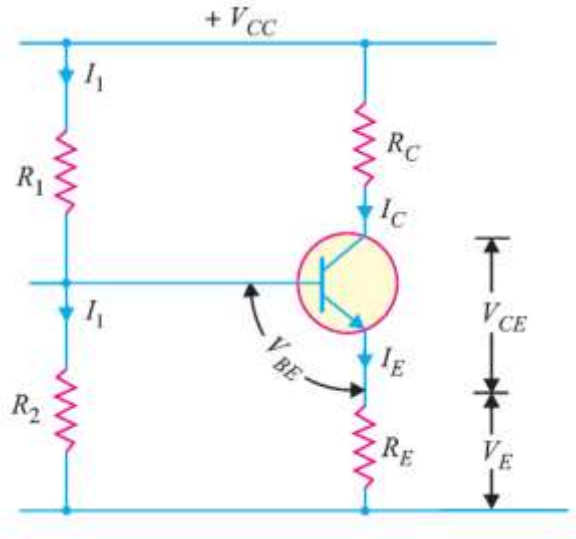
❖ Disadvantages :

(*i*) The circuit does not provide good stabilization because stability factor is fairly high, though it is lesser than that of fixed bias. Therefore, the operating point does change, although to lesser extent, due to temperature variations and other effects.

(*ii*) This circuit provides a negative feedback which reduces the gain of the amplifier as explained hereafter. During the positive half-cycle of the signal, the collector current increases. The increased collector current would result in greater voltage drop across R_C. This will reduce the base current and hence collector current.

Sr no	QUESTION	ANSWER
1.	Collector feedback biasing gives _____thermal stability than fixed biasing.	better
2.	Which biasing method required only one resistance for bias?	Collector feedback resistor
3.	Does operating point change due to temperature variation and other effects?	Yes/True
4.	The stability factor of a collector feedback bias circuit is ..... that of base resistor bias.	Less than

❖ Voltage Divider Bias Method :



Scan here for video

- This is the most widely used method of providing biasing and stabilisation to a transistor. In this method, two resistances R_1 and R_2 are connected across the supply voltage V_{CC} (See above Fig.) and provide biasing.
- The emitter resistance R_E provides stabilisation. The name ‘‘voltage divider’’ comes from the voltage divider formed by R_1 and R_2. The voltage drop across R_2 forward biases the base- emitter junction. This causes the base current and hence collector current flows in the zero signal conditions.

- **Circuit analysis :**

Suppose that the current flowing through resistance R_1 is I_1. As base current I_B is very small, therefore, it can be assumed with reasonable accuracy that current flowing through R_2 is also I_1.

1. Collector current I_C :

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$\therefore$ Voltage across resistance R_2 is

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$$

Applying Kirchhoff's voltage law to the base circuit of Fig.

$$V_2 = V_{BE} + V_E$$

or $$V_2 = V_{BE} + I_E R_E$$

or $$I_E = \frac{V_2 - V_{BE}}{R_E}$$

Since $I_E \simeq I_C$

$\therefore$ $$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \text{.....(i)}$$

- It is clear from exp. (*i*) above that I_C does not at all depend upon β. Though I_C depends upon V_{BE} but in practice $V_2 >> V_{BE}$ so that I_C is practically independent of V_{BE}.
- Thus I_C in this circuit is almost independent of transistor parameters and hence good stabilisation is ensured.
- It is due to this reason that potential divider bias has become universal method for providing transistor biasing.

(*ii*) Collector-emitter voltage V_{CE} :

Applying Kirchhoff's voltage law to the collector side,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + I_C R_E \qquad (\because I_E \simeq I_C)$$

$$= I_C (R_C + R_E) + V_{CE}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Stabilization. In this circuit, excellent stabilization is provided by R_E. Consideration of eq. (*i*) reveals this fact.

$$V_2 = V_{BE} + I_C R_E$$

Suppose the collector current I_C increases due to rise in temperature. This will cause the voltage drop across emitter resistance R_E to increase. As voltage drop across R_2 (*i.e.* V_2) is *independent of I_C, therefore, V_{BE} decreases. This in turn causes I_B to decrease. The reduced value of I_B tends to restore I_C to the original value.

Stability factor: It can be shown mathematically that stability factor of the circuit is given by:

$$\text{Stability factor, } S = \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E + \beta R_E}$$

$$= (\beta + 1) \times \frac{1 + \dfrac{R_0}{R_E}}{\beta + 1 + \dfrac{R_0}{R_E}}$$

$$\text{where } R_0 = \frac{R_1 R_2}{R_1 + R_2}$$

If the ratio R_0/R_E is very small, then R_0/R_E can be neglected as compared to 1 and the stability factor becomes :

$$\text{Stability factor} = (\beta + 1) \times \frac{1}{\beta + 1} = 1$$

This is the smallest possible value of S and leads to the maximum possible thermal stability. Due to design **considerations, R_0 / R_E has a value that cannot be neglected as compared to 1. In actual practice, the circuit may have stability factor around 10.

Sr no	QUESTION	ANSWER
1.	The disadvantage of voltage divider bias is that it has _____.	Many resistors
2.	Stability factor value of voltage divider bias method is _____.	1
3.	Smallest possible value of stability factor leads to the _____ possible thermal stability.	Maximum
4.	Two resistance connected across the supply voltage is known as _____ biasing .	Voltage divider

❖ Chapter Review Topics:

1. What is faithful amplification? Explain the conditions to be fulfilled to achieve faithful amplification in a transistor amplifier.

2. What do you understand by transistor biasing? What is its need?

3. What do you understand by stabilization of operating point?

4. Mention the essentials of a biasing circuit.

5. Describe the various methods used for transistor biasing. State their advantages and disadvantages.

6. Write short notes on the following :

(i) Operating point (ii) Stabilization of operating point.