

# SHREE H. N. SHUKLA GROUP OF COLLEGES

(Affiliated to Saurashtra University & Gujarat Technological University)



2 – Vaishalinagar

Nr. Amrapali Railway Crossing

Raiya Road

Rajkot – 360001

Ph.No–(0281)2440478,2472590

3 – Vaishalinagar

Nr. Amrapali Railway Crossing

Raiya Road

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Ph.No–(0281)2471645

## C.O.A

### QUESTION BANK

#### CH-1: DIGITAL LOGIC CIRCUIT.

#### 2 MARKS QUESTION

NO	QUESTION
1.	WHAT IS LOGIC GATE?
2.	WHAT IS BOOLEAN ALGEBRA?
3.	WHAT IS TRUTH TABLE?
4	WHAT IS UNIVERSAL GATE?

#### 3MARKS QUESTION

1	EXPLAIN DON'T CARE CONDITION.
2	WHAT IS BOOLEAN FUNCTION?
3	WHAT IS CLOCK PULSE?
4	WHAT IS K'MAP?
5	EXPLAIN POSTULATES.

#### 5MARKS QUESTION

1	EXPLAIN GATE.
2	EXPLAIN K'MAP4 VARIABLE

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<u>3</u>	EXPLAIN FLIP FLOP.
<u>4</u>	EXPLAIN HALF ADDER AND FULL ADDER.
<u>5</u>	EXPLAIN SEQUENTIAL CIRCUIT.

## CH-2: DIGITAL COMPONENT.

2MARKS

<u>1</u>	EXPLAIN INTEGRATED CIRCUIT.
<u>2</u>	EXPLAIN COUNTER.
<u>3</u>	EXPLAIN REGISTER.
<u>4</u>	EXPLAIN SHIFT REGISTER.

3MARKS.

<u>1</u>	EXPLAIN MUX.
<u>2</u>	EXPLAIN DE-MUX.
<u>3</u>	EXPLAIN 4BIT BINARY COUNTER.
<u>4</u>	EXPLAIN ACHRONOUS COUNTER.

5MARKS.

<u>1.</u>	EXPLAIN DECODER
<u>2</u>	EXPLAIN ENCODER.
<u>3</u>	EXPLAIN 2*8 DECODER.

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## CH-3: DATA REPRESENTATION.

2MARKS

<u>1</u>	EXPLAIN BINARY ADDITION
<u>2</u>	EXPLAIN BINARY MULTIPLICATION
<u>3</u>	EXPLAIN 1'S COMPLEMENT
<u>4</u>	EXPLAIN 2'S COMPLEMENT

3MARKS

<u>1</u>	EXPLAIN FIXED POINT REPRESENTATION
<u>2</u>	EXPLAIN FLOATING POINT REPRESENTATION
<u>3</u>	EXPLAIN PARITY BIT
<u>4</u>	EXPLAIN ERRORCORRECTION CODE.

5MARKS

<u>1</u>	EXPLAIN ERROR DETECTION CODE.
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## CH-4: CPU

2MARKS

<u>1</u>	WHAT IS CPU?
<u>2</u>	EXPLAIN ALU.
<u>3</u>	EXPLAIN POLISH NOTATION
<u>4</u>	EXPLAIN RPN.

3MARKS

<u>1</u>	EXPLAIN MAJOR COMPONENT OF CPU.
<u>2</u>	EXPLAIN STACK.
<u>3</u>	EXPLAIN CONTROLWORD.
<u>4</u>	EXPLAIN AC REGISTER.

5MARKS

<u>1</u>	EXPLAIN ALU IN DETAIL
<u>2</u>	EXPLAIN GENERAL REGISTER ORG.
<u>3</u>	EXPLAIN INTERRUPT.

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## CH-5: I/O ORGANIZATION

2MARKS

1	WHAT IS MEMORY BUS ?
2	EXPLAIN BUS.
3	EXPLAIN DATA BUS
4	EXPLAIN CONTROL BUS

3MARKS

1	Block DIAGRAM OF MEMORY BUS
2	BLCIOK DIAGRAM OF DATA BUS
3	I.O.P
4	EXPLAIN I.O.INTERFACE

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5 MARKS

<u>1</u>	EXPLAIN DMA
<u>2</u>	EXPLAIN WORKING OFDMA
<u>3</u>	EXPLAIN DMACONTROLLER.

