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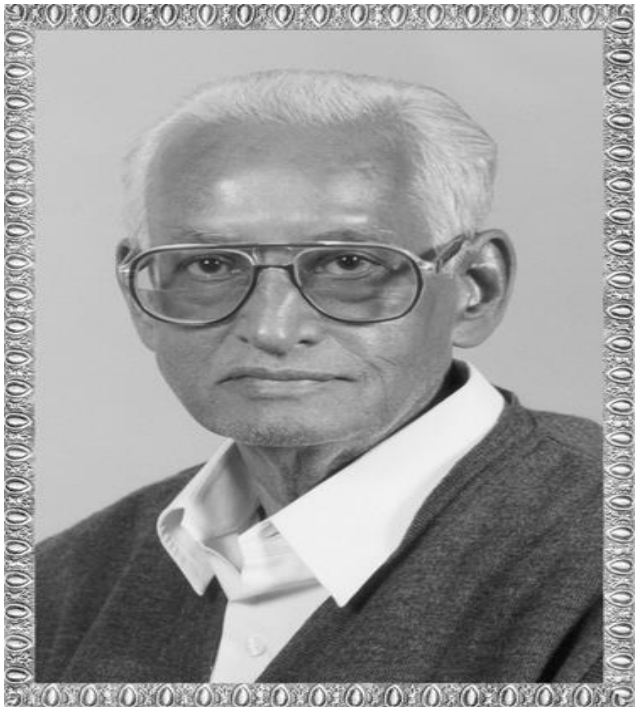

Lt. Shree Chimanbhai Shukla

B.C.A./B.Sc.IT-SEMESTER-2

SUB :- COMPUTER ORGANIZATION & ARCHITECTURE

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CH-1 DIGITAL LOGIC CIRCUIT
14 MARKS
22 LECTURES

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Q-1 WHAT IS DIGITAL COMPUTER?

DETAILING:

- Digital computer is machine that store data in **numerical format**.
- Digital computer use **binary number system.**
- The first digital computer was developed **in 1940**.

☑ One Marks Questions:- ☑

Question	Answer
1. Digital computer use ___	Binary number system
2. When was found first digital computer?	1940

Q-2 WHAT IS LOGIC GATE? EXPLAIN TYPES OF LOGIC GATE.

DETAILING:

☐LOGIC GATE:

- The **calculation** of **binary information** is done by **logic circuit** is called logic gate.
- Gate is electronics circuit with **one or more** input **but** only **one output.**
- Each gate has **logic circuit , Boolean function and truth table**.
- There are three types of logic gate

1. **Basic Gate**
2. **Universal Gate**
3. **Exclusive Gate**

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Basic Gate:-

- Basic gate has **4** sub gates like **And , Or , Not , Buffer.**
- Now we explain each and every basic gates.

☆1)AND Gate:-

- The and gate produce the and logic circuit.
- The and gate is used for multiplication.

☑ Logic circuit/ Boolean circuit:-

☑ Boolean function:- C= A.B OR C=(AB)

☑ Truth table:-

A	B	C(AB)
0	0	0
0	1	0
1	0	0
1	1	1

- In above diagram there are **two input** like **A** and **B** . and there is only **one output** is **C.**

- in the truth table output is **one** when **both** input are **one** otherwise **output** will be **zero.**

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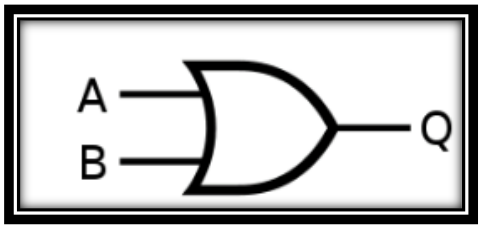
☆2) OR Gate:-

- The or gate produce the **or logic circuit.**
- The or gate is used **for addition.**

☑ Logic circuit/ Boolean circuit:-



☑ Boolean function:- **C= A+B** **OR** **C=(A+B)**

☑ Truth table:-

A	B	C(A+B)
0	0	0
0	1	1
1	0	1
1	1	1

- In above diagram there are **two input** like **A** and **B** . and there is only **one output** is **C.**

- in the truth table output is **zero** when **both** input are **Zero** otherwise **output** will be **one.**

☆3) NOT Gate:-

- The not gate is also called **inverter gate** , **compliment** gate and **reverse** gate.

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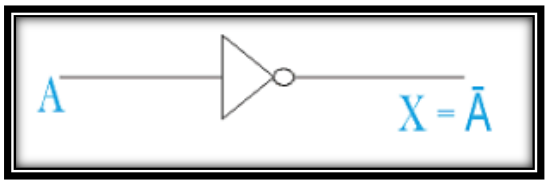
☑ **Logic circuit/ Boolean circuit:-**



☑ **Boolean function:-** **A= A' OR A=A**

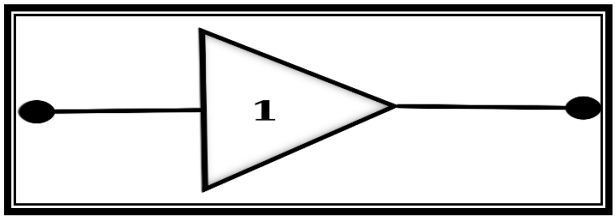
☑ **Truth table:-**

A	A
0	1
1	0

- Not gate is **compliment** gate.
- It has only one **input** and **one output.**

☆4)Buffer Gate:-

☑ **Logic circuit/ Boolean circuit:-**



☑ **Boolean function:-** **A= A OR A=A**

☑ **Truth table:-**

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A	A
0	0
1	1

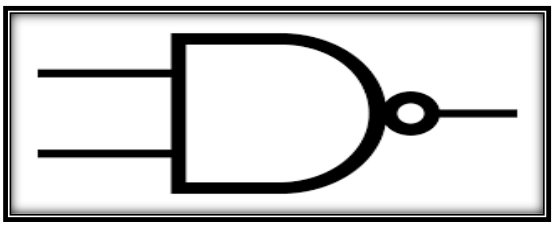
Universal Gate:-

- There are **two types** of universal gate like **nand and nor**.
- Nand means **negative and ,nor means negative or**.
- Universal gate is compliment gate of basic gate.
- Why are they called universal gates?
- NAND and NOR gates are called universal gates **because** they **perform all the Logic functions OR, AND and NOT.**

☆1) Nand Gate:-

- The nand gate is **negative** of **and gate.**
- The nand gate is **universal gate.**
- The nand gate has **two input** and **only one output**.
- The nand gate is **complement** of **and gate**.

☑ Logic circuit/ Boolean circuit:-



☑ Boolean function:- $C=\overline{(A.B)}$ OR $C=(\overline{A}B)$

☑ Truth table:-

A	B	$C(\overline{AB})$
0	0	1

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0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

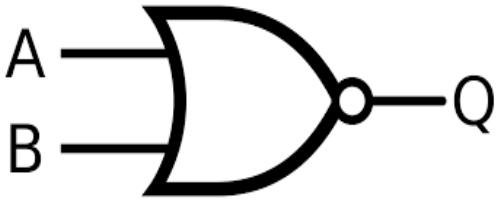
- In above diagram there are **two input** like **A** and **B** . and there is only **one output** is **C.**

- in the truth table output is **zero when both input are one**. Other wise **output will be 1.**

☆2) Nor Gate:-

- The nor gate means **negative or**
- It is **compliment** of or gate.
- The nor gate is **reverse of or gate.**

☑ Logic circuit/ Boolean circuit:-



☑ Boolean function:- $C=\overline{(A+B)}$ **OR** $C=(\overline{A}+B)$

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☑ **Truth table:-**

A	B	C(A+B)
0	0	1
0	1	0
1	0	0
1	1	0

- In above diagram there are **two input** like **A** and **B** . and there is only **one output** is **C.**
- in the truth table output is **one when both input are zero**. Other wise **output will be zero.**

Exclusive Gate:-

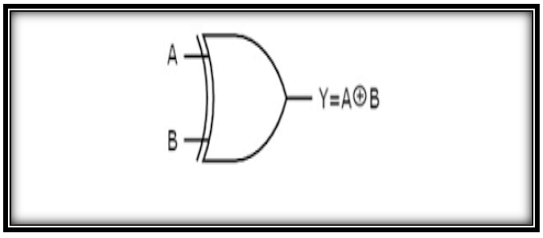
- there are two types of exclusive gate like **ex-or** and **ex-nor**.

- Now we can explain both gate one by one.

☆1) Exclusive Or Gate:-

- The exclusive or gate is also **called Xor gate.**

☑ **Logic circuit/ Boolean circuit:-**



☑ **Boolean function:-** **C= (A + B)**

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☑ **Truth table:-**

A	B	C(A ⊙ B)
0	0	0
0	1	1
1	0	1
1	1	0

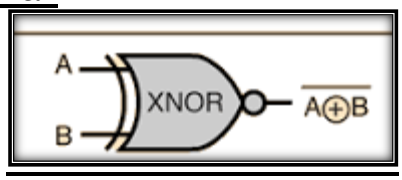
- In above diagram there are **two input** like **A** and **B** . and there is only **one output** is **C.**

- in the truth table output is **zero when both input are same**. Other wise **output will be one.**

☆2) Exclusive NOr Gate:-

- The exclusive Nor gate is also **called Ex nor gate.**
- It is **compliment** of **ex or gate**

☑ **Logic circuit/ Boolean circuit:-**



☑ **Boolean function:-** $C = \overline{(A + B)}$

☑ **Truth table:-**

A	B	C(A ⊙ B)
0	0	1
0	1	0
1	0	0
1	1	1

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- In above diagram there are **two input** like **A** and **B** . and there is only **one output** is **C.**

- in the truth table output is **one when both input are same**. Other wise **output will be zero.**

☑ One Marks Questions:- ☑

Question	Answer
1. how many types of gate are available?	8
2. give the name of basic gate	And , or , not.
3. Nor means?	Negative or
4. Nand mens?	Negative and.
5. Ex or means?	Exclusive or.

Q-3 WHAT IS BOOLEAN VARIABLE?

DETAILING:

- A variable that consist only **two** values either **o and 1** is known as **Boolean variable** or **binary variable**.
- The valid binary variable name are **a, b** , **A , B** , **a1 , a2** etc.

Q-4 WHAT IS TRUTH TABLE ?.

DETAILING:

- The table which represent **relationship** between **variable** and **function** is known as **truth table**.

Q-5 DRAW THE LOGIC CIRCUIT FOR THE FOLLOWING FUNCTION ?.

DETAILING:

1) **F= ABC**

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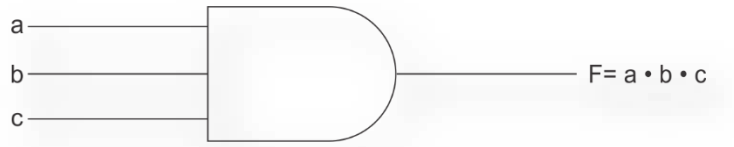
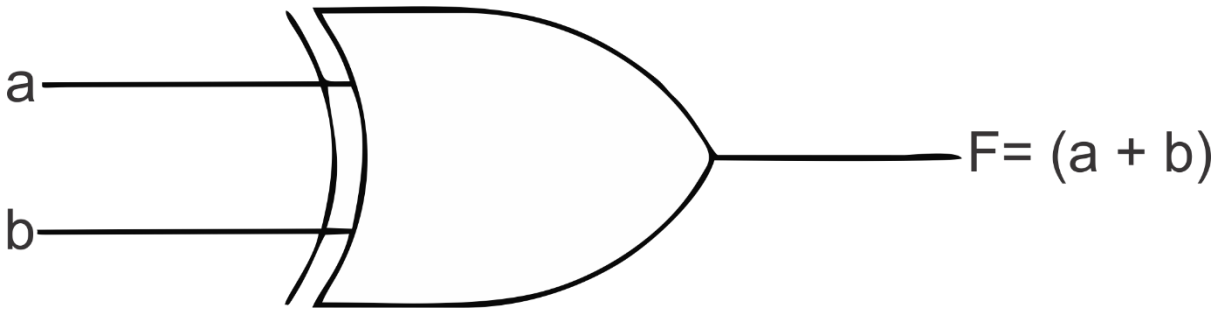
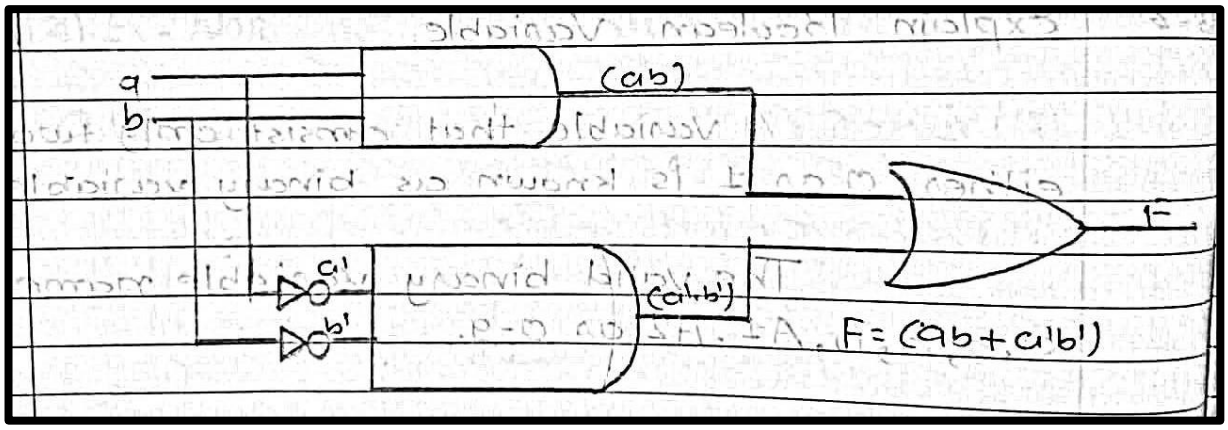


2) F= (a b)



3) F= (ab + a'b')



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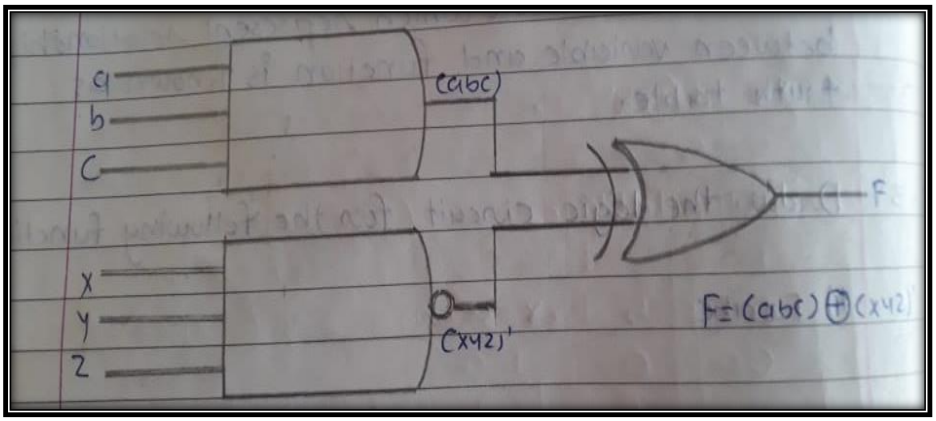
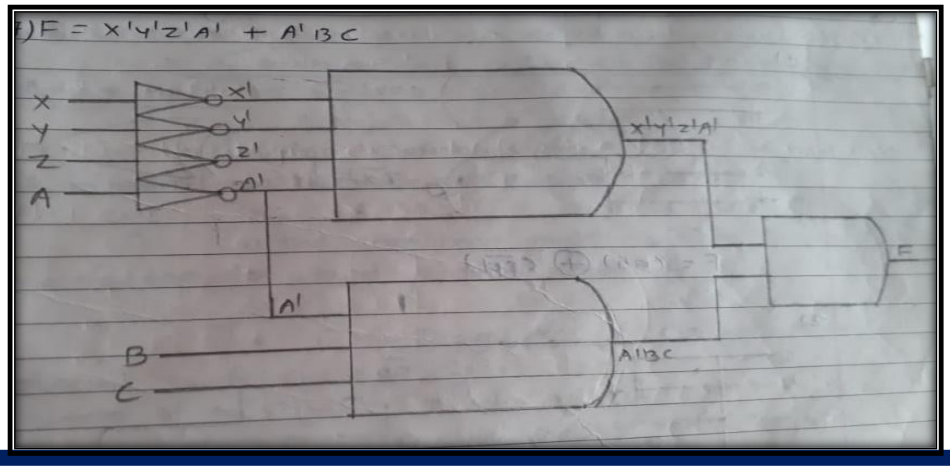
4)



5)



Q-6 GIVE THE EQUATION FOR FOLLOWING CIRCUIT .

DETAILING:

1)

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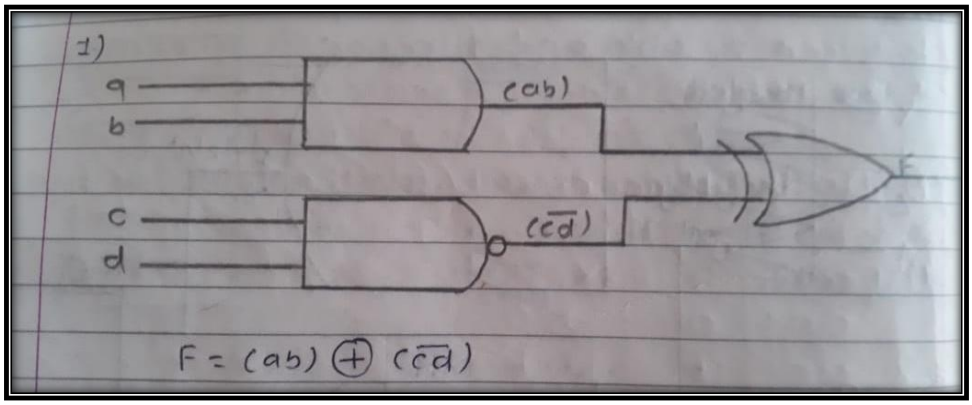
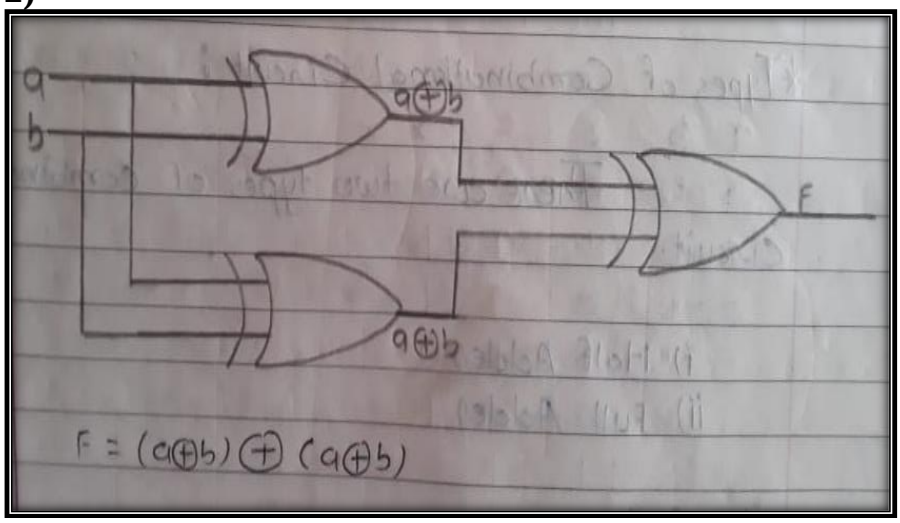


2)



Q-7 EXPLAIN COMBINATIONAL CIRCUIT AND EXPLAIN ITS TYPES.

DETAILING:

- Combinational circuit is **collection of logic gate.**
- In the combinational circuit there is **no future to store previous output**.
- in the combinational circuit **output** is **depend** on **the basic current input**
- the block diagram of combinational circuit is follow.

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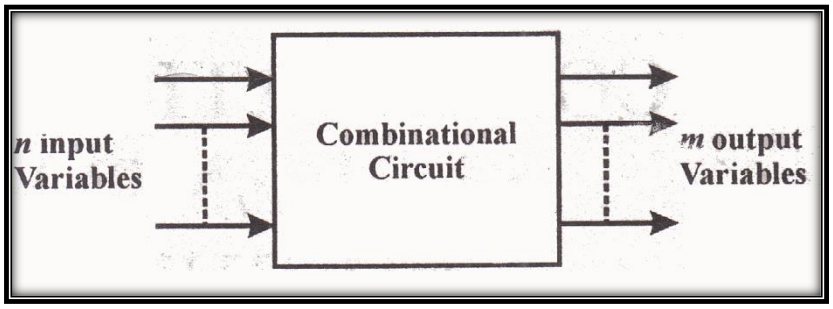


- In the above diagram there are **n input** and **m output** variable.
- If there are **n input** so we can **get 2^n output.**

➔ Types of combinational circuit:-

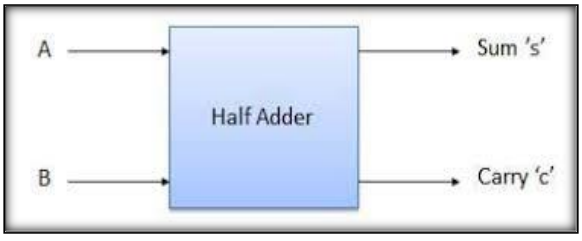
- There are **two types** of combinational circuit like
  1) **Half adder and 2) full adder**.

☆1) Half adder:-

☑ a combinational circuit that **perform** binary **addition** of **two bits** are called half adder.

☑ the input variable of half adder are called **augend** and **adder**.

☑ Block diagram of half adder are follow.



☑ in the above diagram there are **two** input like **a** and **b** and there are **two output** like **s** and **c.**

☑ **s** means **sum** and **c** means **carry.**

☑ **Truth table:-**

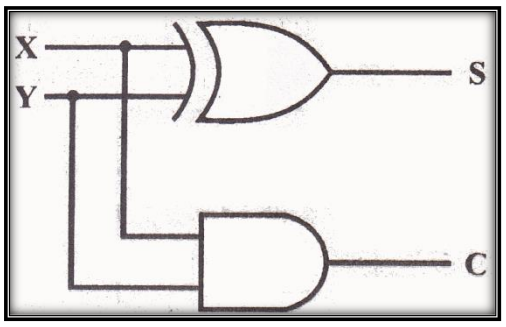
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

☑ **Boolean function:-**

S= a ⊕ b

C= ab

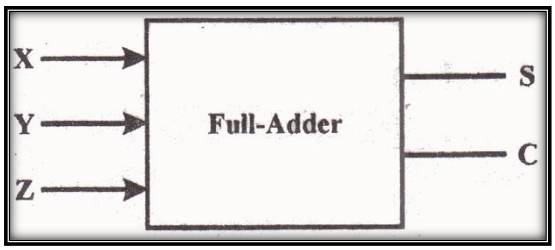
☑ **Logic circuit/ Boolean circuit:-**



☆2) **Full adder:-**

☑ a combinational circuit that perform binary addition of three or more bits is known as full adder.

☑ a block diagram of combinational circuit is follow.



☑ **Truth table:-**

X	Y	Z	C	S
0	0	0	0	0

0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

☑ One Marks Questions:- ☑

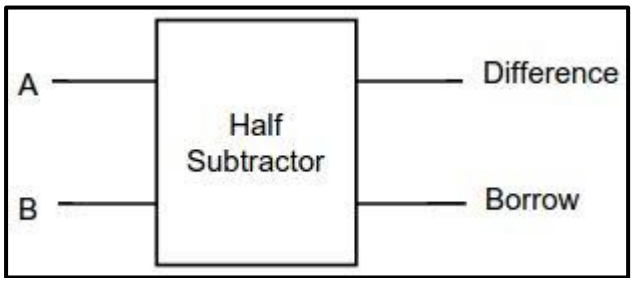
Question	Answer
1. Ha means___	Half adder
2. Fa means___	Full adder
3. Half adder add___ bits	2
4. Full adder add ___bits	3 or more
5. C means___	Carry

Q-8 EXPLAIN HALF SUBTRACTOR AND FULL SUBTRACTOR.

DETAILING:

☆1) Half subtractor:-

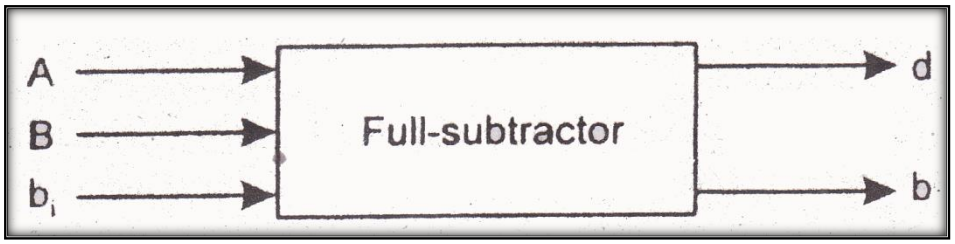
☑ A combinational circuit that perform binary **subtraction** of **two bits** is knows as **half subtractor**.
☑ block diagram of half subtractor is follow.



☑ in the above diagram there are **two input** like A and B. and there are **two output** like **d** and **b**. d means **difference** and b means **borrow.**

☆2) Full subtractor:-

☑ A combinational circuit that perform binary **subtraction** of **three or more bits** is knows as **Full subtractor**.
☑ block diagram of half subtractor is follow.



☑ in the above diagram there are **three input** like A and B and b. and there are **two output** like **d** and **b**. d means **difference** and b means **borrow.**

☑ One Marks Questions:- ☑

Question	Answer
1. Hs means___	Half subtractor
2. Fs means___	Full subtractor
3. Half subtractor minus___ bits	2
4. Fs minus ___bits	3 or more
5. D means___	difference

Q-9 EXPLAIN MIN TERM OR EXPLAIN SUM OF PRODUCT(SOP) OR. EXPLAIN STANDARD PRODUCT.

DETAILING:

☑ **Consider** if we have **two** binary **variable** like **A** and **B.**

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☑ if we perform **And** operation**(*)** between this two variable , so we can get **four** unique combination this combination is called is **min term**.
☑ in min term **always** use **And** gate.
☑ **two** variable min term as per follow.

A	B	Min Term	Designation
0	**0**	**A' B'**	**Mo**
0	**1**	**A' B**	**M1**
1	**0**	**A B'**	**M2**
1	**1**	**A B**	**M3**

☑ **three** variable min term as per follow.

Input			Min Terms (Standard product terms)	Min Term Designation
X	Y	Z		
0	0	0	X' Y' Z'	m_0
0	0	1	X' Y' Z	m_1
0	1	0	X' Y Z'	m_2
0	1	1	X' Y Z	m_3
1	0	0	X Y' Z'	m_4
1	0	1	X Y' Z	m_5
1	1	0	X Y Z'	m_6
1	1	1	X Y Z'	m_7

☑ Min term are also **known** as **standard product**.
☑ The **symbol** of min term is **"mi"**

☑ One Marks Questions:- ☑

Question	Answer
1. Min term use___ gate	And
2. Sop means ___	Sum of product
3. Symbol of min term is__	"mi"

Q-10 EXPLAIN MAX TERM OR EXPLAIN PRODUCT OF SUM(POS) OR. EXPLAIN STANDARD SUM.

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DETAILING:

☑ **Consider** if we have **two** binary **variable** like **A** and **B.**
☑ if we perform **OR** operation**(+)** between this two variable , so we can get **four** unique combination this combination is called is **max term**.

A	B	Max Term	Designation
0	**0**	**A + B**	**Mo**
0	**1**	**A + B'**	**M1**
1	**0**	**A'+ B**	**M2**
1	**1**	**A'+ B'**	**M3**

☑ **three** variable max term as per follow.

Input			MaxTerms	max Term Designation
X	Y	Z		
0	0	0	X + Y + Z	m_0
0	0	1	X + Y + Z'	m_1
0	1	0	X + Y' + Z	m_2
0	1	1	X + Y' + Z'	m_3
1	0	0	X + Y + Z	m_4
1	0	1	X' + Y + Z'	m_5
1	1	0	X' + Y' + Z	m_6
1	1	1	X' + Y' + Z'	m_7

☑ Max term are also **known** as **product of sum**
☑ The **symbol** of max term is **"Mi"**

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Q-11 EXPLAIN K'MAP.(KARNAUGH MAP)

DETAILING:

☑ K'map is **mapping** method to **simplify** **Boolean function.**
☑ K'map is **mapping** method **which describe** **min term** into **graphical format**.
☑ there are **three types** of k'map like **two** variable , **three** variable and **four** variable k'map.

1) two variable k'map:-
☑ consider that kmap for two variable now we can describe follow

Mo	M1
M2	M3

O	**1**
2	**3**

00	**01**
10	**11**

A'b'	**A'b**
AB'	**AB**

☑EX-1:-

1) F=(A,B)= <(0,2) Solve using k' map.

Mo	M1
M2	M3

O	
2	

00	
10	

A'b'	
Ab'	

Ans f=b'.

2) three variable k'map:-

☑ consider that kmap for three variable now we can describe follow

Mo	M1	M3	M2
M4	M5	M7	M6

O	1	3	2
4	5	7	6

X \ YZ	00	01	11	10
0	X'Y'Z'	X'Y'Z	X'Y Z	X'Y Z'
1	X Y'Z'	X Y'Z	X Y Z	X Y Z'

3) four variable k'map:-

☑ consider that kmap for four variable now we can describe follow

WX \ YZ	00	01	11	10
00	W'X'Y'Z' 0	W'X'Y'Z 1	W'X'Y Z 3	W'X'Y Z' 2
01	W'X Y'Z' 4	W'X Y'Z 5	W'X Y Z 7	W'X Y Z' 6
11	W X Y'Z' 12	W X Y'Z 13	W X Y Z 15	W X Y Z' 14
10	W X'Y'Z' 8	W X'Y'Z 9	W X'Y Z 11	W X'Y Z' 10

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Ex. F (a, b, c, d) = E (12, 2, 14, 10)

m0	m1	m3	m2
m4	m5	m7	m6
m12	m13	m15	m14
m8	m9	m11	m10

0	1	3	**2**
4	5	7	6
12	13	15	**14**
8	9	11	**10**

0000	0001	0011	**0010**
0100	0101	0111	0110
1100	1101	1111	**1110**
1000	1001	1011	**1010**

-	-	-	**ab**c**d**
-	-	-	-
ab**cd**	-	-	Abc**d**
-	-	-	a**b**c**d**

Ans. F= d

☑ One Marks Questions:- ☑

Question	Answer
1. Full form of k ‘ map	Karnaugh map

Q.12 EXPLAIN DON’T CARE CONDITION.

DETAILING:

☑ In Kmap every call represent a **min- term(max- term)** means **0 ro1** but we **don’t care** about **0 or 1**, this condition is called Don’t care condition.

Ex. F(a, b)=*Σ*(1, 2)+d(0, 3)

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0	1
2	3

X	1
2	X

Q.13 EXPLAIN SEQUENTIAL CIRCUIT (2- MARK)

DETAILING:

☑ In the sequential circuit **output** is **depend** on the basic **input** as well as **previous output**.
☑ In the sequential circuit there is **future to store** previous **output**.

☆ **Types of Sequential Circuit or**
Explain Flip- Flop. Or
Explain Latch.

☑ Flip- Flop is **Binary cell** cable of **store 1-bit** information.
☑ Flip Flop is **Sequential Circuit.**
☑ It can store **binary bit.**
☑ It is also called **Latch.**
☑ Flip- Flop was found in **1919** by **William Eccles and F. W. Jordon.**
☑ It is called **Eccles- Jorden trigger circuit**.

☆ **Type of Flip- Flop**

☑ There 5 type of Flip- Flop.

1. SR Flip- Flop
2. D Flip- Flop
3. T- Flip- Flop
4. J- K Flip- Flop
5. Master Slave Flip- Flop

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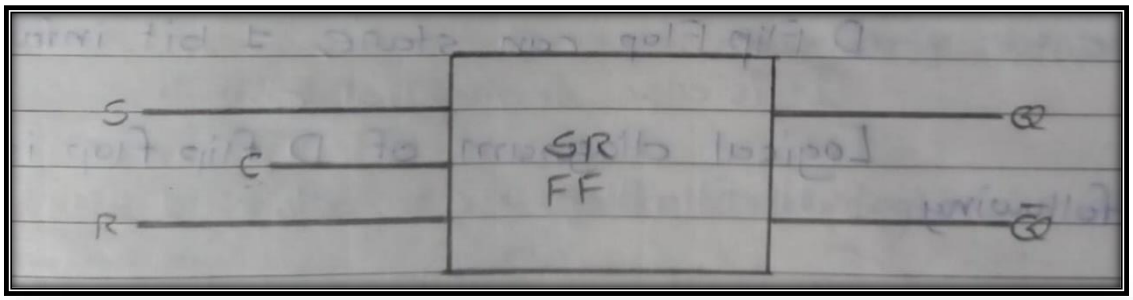
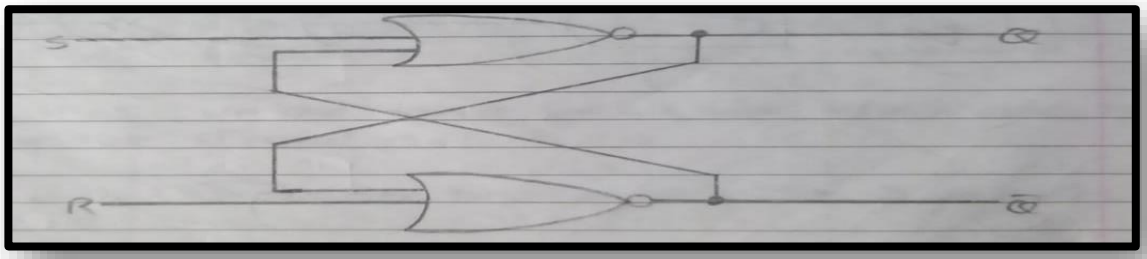
☆ 1) SR Flip- Flop(Set and Reset)

Block diagram of SR Flip- Flop is Follow

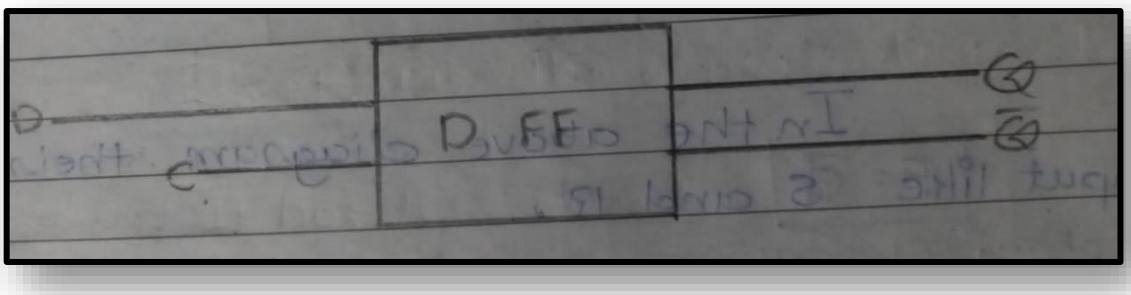




☑ In the above diagram there are **two** input like **S** and **R**
☑ One addition **input is C.**
☑ There are two **output** like **Q & $\bar{Q}$.**
☑ SR Flip- Flop can **store 1-bit** memory.
☑ Logic Circuit of SR Flip- Flop is Following.

☆ 2) D Flip- Flop(Data filp flop):-

☑ D Flip- Flop is **sequential Circuit**.

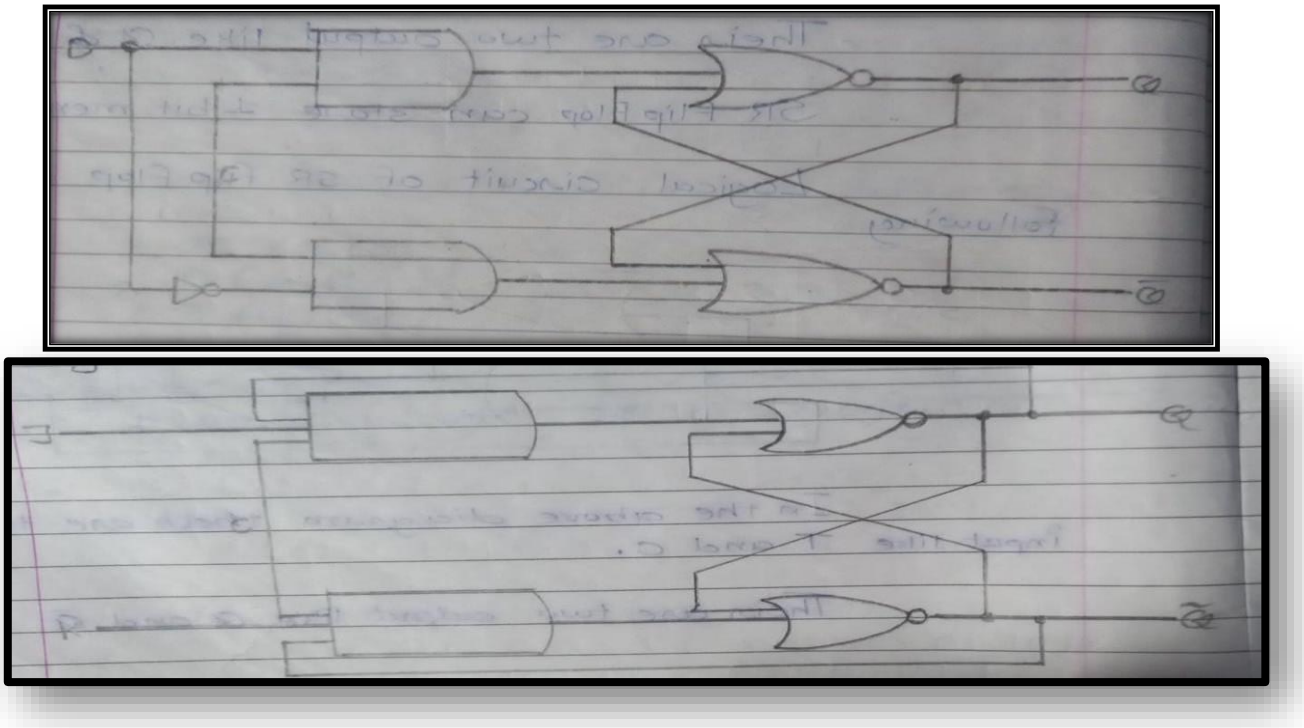


☑ D Flip- Flop can **store 1 bit** information.
☑ Logic diagram of D Flip- Flop is Following.

Logic Circuit

☆ **3) T Flip- Flop(Toggle):-**

☑ T Flip- Flop is **Sequential Circuit**.



☑ T Flip- Flop can **store only one** bit information **at a time.**
☑ Block Diagram and Logic circuit of T Flip- Flop is follow.
☑ In the above diagram there are two input like T and C.
☑ There are two out put like Q and $\bar{Q}$.

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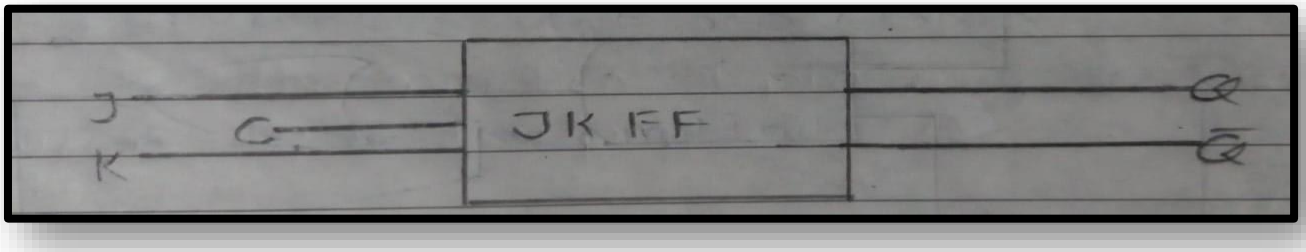
☆ 4) JK Flip- Flop:-

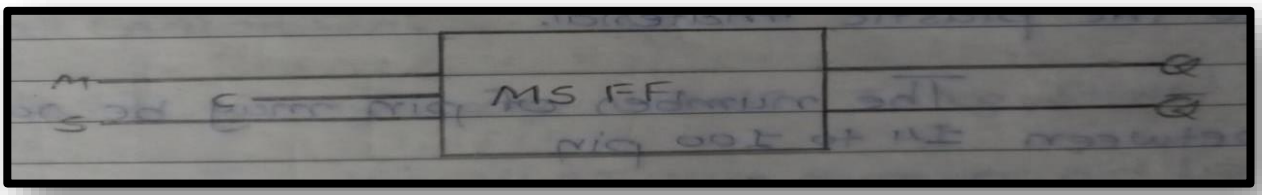
☑ JK Flip- Flop is also called Jump and Kick Flip- Flop.
☑ It is also sequential circuit.
☑ JK Flip- Flop use to store 1 bit information .
☑ JK Flip- Flop has three input Like J, K and C.
☑ It has two output.
☑ Block Diagram and Logic Circuit of JK Flip- Flop is as follow:



☆ 5) Master Slave Flip- Flop:-

☑ Master Slave Flip- Flop is a sequential circuit
☑ Master Slave Flip- Flop are use to store 1 bit information.
☑ Master Slave Flip- Flop two input like Master and Slave.
☑ One addition output is C.

BLOCK DIAGRAM



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☑ There are two output like Q and $\bar{Q}$.

☑ One Marks Questions:- ☑

Question	Answer
1. FF MEANS ___	FLIP FLOP
2. RS FLIP FLOP MEANS	SET AND RESET FLIP FLOP
3. FLIP FLOP CAN STORE ___ BIT	1 BIT
4. JK MEANS___	JUMP AND KICK FLIP FLOP

Q.14 EXPLAIN CLOCK PULSE .

DETAILING:

☑ It is a circuit **located** inside the computer that **help increase** the speed of computer.

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CHAPTER- 2 DIGITAL COMPONENT
14 MARKS
22 LECTURES

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Q-1 EXPLAIN I. C.

DETAILING:

☑ Integrated Circuit called **IC**, **Micro Circuit**, **Micro Chip**, **Silicon Chip** or **chip**
☑ Integrated Circuit are **use** in almost **electronic device today**.
☑ Integrated Circuit are **collection** of **Interconnected logic Gate**.
☑ To **supply** and **generate output** in the integrated circuit, **external pin are interconnected** to the plastic material.
☑ The **number** pin may be **range** in between **14 to 100 pin.**
☑ **There are various type of I. C. available like.**

- **SSI** (SMALL SCALE INTREGATION)
- **MSI** (MEDIUM SCALE INTREGATION)
- **LSI** (LARGE SCALE INTREGATION)
- **VLSI** (VERY LARGE SCALE INTREGATION)
- **ULSI** (ULTRA LARGE SCALE INTREGATION)

1. SSI (SMALL SCALE INTREGATION)

☑ In the SSI the number of **logic gates** are approx. **less than or equal to 10.**
☑ Generally, this **logic gate** is **Independent.**

2. MSI (MEDIUM SCALE INTREGATION)

☑ In the MSI either number of logic gates are approx. **in between 10 to 20.**
☑ MSI is more **complex** then **SSI**.

3. LSI (LARGE SCALE INTREGATION)

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☑ In lxi number of logic gates are **between 200 to 1000.**
☑ LSI it is more **complex then SSI**.
☑ **Example** of LSI is **PEROM and small Processor.**

4. VLSI (VERY LARGE SCALE INTREGATION)

☑ In the VLSI the number of **logic gates** are **more than 1 Lack.**
☑ The example of VLSI is **microchip** of computer.

5. ULSI (ULTRA LARGE SCALE INTREGATION)

☑ In the ULSI the number of logic gates are more than 1 million.

☑ One Marks Questions:- ☑

Question	Answer
1. IC MEANS___	INTEGRATED CIRCUIT
2. SSI MEANS	SMALL SCALE INTEGRATION
3. MSI MEANS	MEDIUM SCALE INTEGRATION
4. ULSI MEANS	ULTRA LARGE SCALE INTEGRATION

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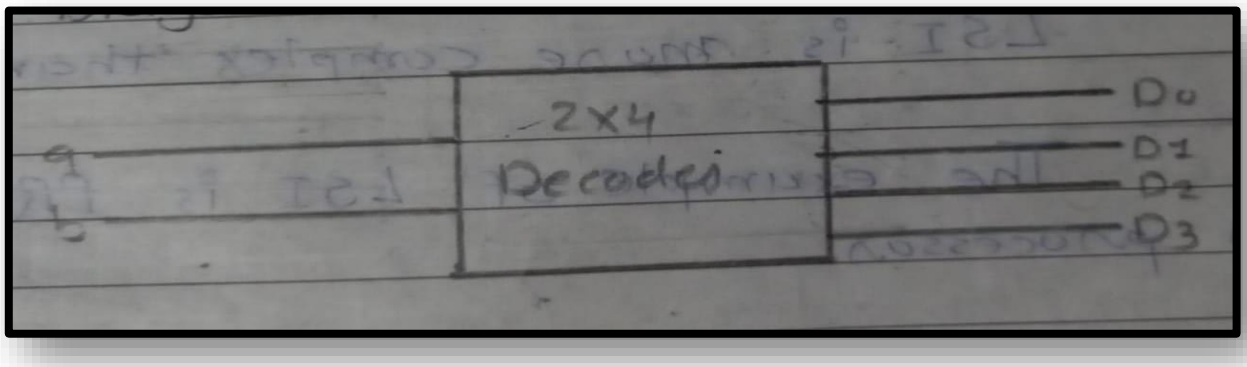
Q-2 EXPLAIN 2 X 4 LINE DECODER.

DETAILING:

☑ Decoder is **logic circuit**.
☑ Decoder convert **n bit** input data **into 2n output** data.
☑ Decoder **convert** **binary language** into **Human readable form.**

Block Diagram



Truth Table

	a	b	D_3	D_2	D_1	D0
$\bar{a} \cdot \bar{b}$	0	0	0	0	0	1
$\bar{a} \cdot b$	0	0	0	0	1	0
$a \cdot \bar{b}$	1	0	0	1	0	0
$a \cdot b$	1	1	1	0	0	0

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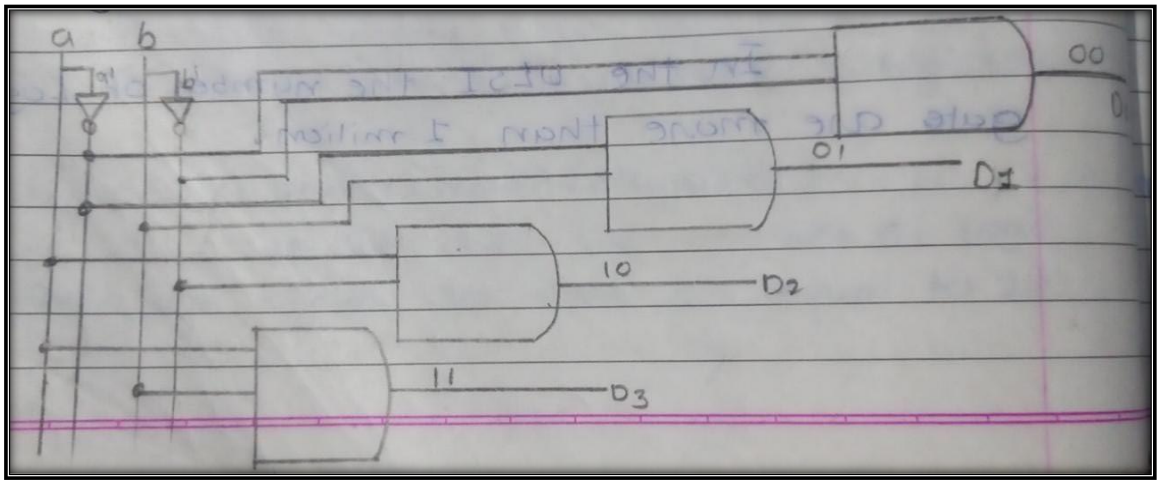
Logic Circuit



☑ One Marks Questions:- ☑

Question	Answer
1. 2*4 means	2 INPUT AND 4 OUTPUT
2. DECODER MEANS__	BINARY TO HUMAN LANGUAGE

Q 3 EXPLAIN 3 X 8 DECODER.

DETAILING:

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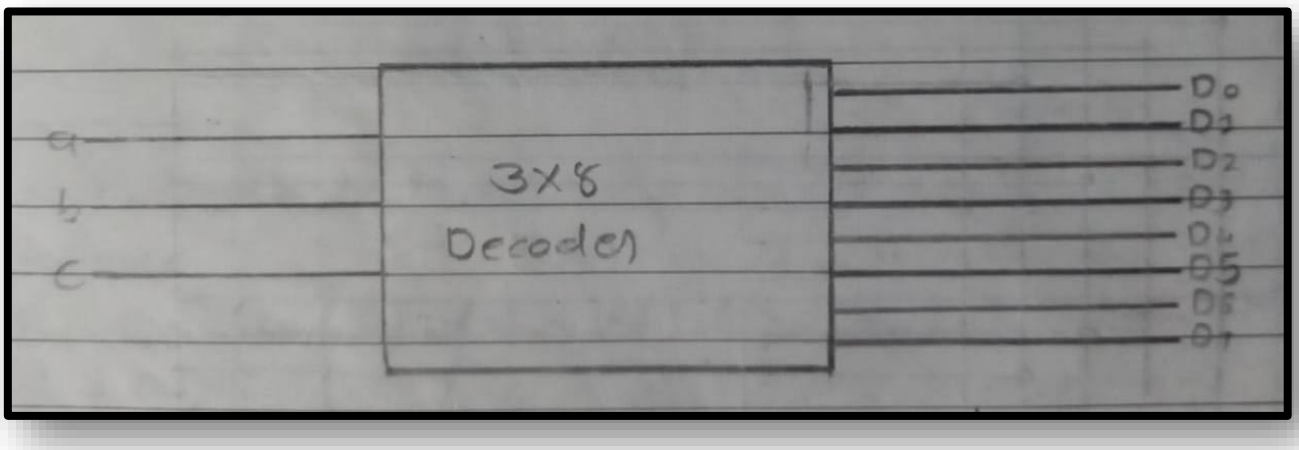
☑ Decoder is **combination circuit.**
☑ Decoder **convert one type** of coded information **into another type**
☑ Decoder **convert binary language into human readable form.**

Block Diagram



Truth Table

	A	B	C	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0	0	0	1
	0	0	1	0	0	0	0	0	0	1	0

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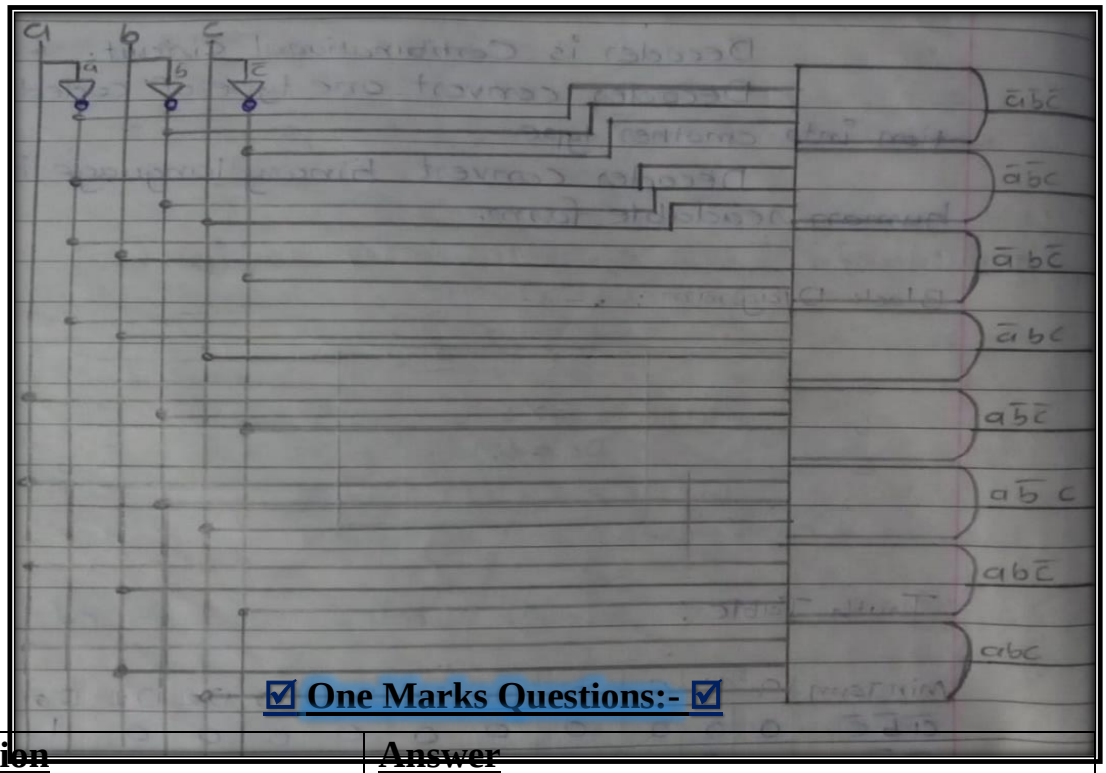
	0	1	0	0	0	0	0	0	1	0	0
	0	1	1	0	0	0	0	1	0	0	0
	1	0	0	0	0	0	1	0	0	0	0
	1	0	1	0	0	1	0	0	0	0	0
	1	1	0	0	1	0	0	0	0	0	0
	1	1	1	1	0	0	0	0	0	0	0

Logic Circuit



☑ One Marks Questions:- ☑

Question	Answer
1. 3*8 means	3 INPUT AND 8 OUTPUT
2. DECODER MEANS__	BINARY TO HUMAN LANGUAGE

Q-4 Explain Encoder.
Explain 4 x 2 Line Encoder

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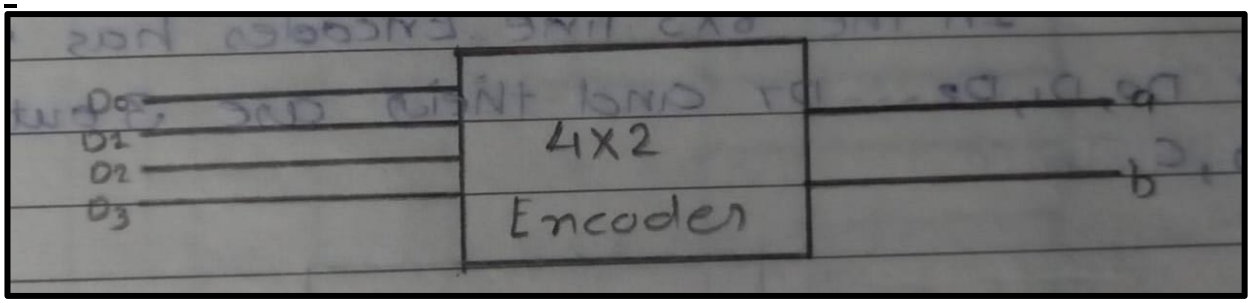
DETAILING:

☑ Encoder **is combinational circuit.**
☑ Encoder is **opposite process of decoder**.
☑ Encoder convert **one type of** coded information to **another type of code**.
☑ Encoder convert **human language into binary language**
☑ There are **two type of encoder**.

1. **4 x 2 line Encoder**
2. **8 x 3 line Encoder**

Block Diagram

`



☑TRUTH TABLE

D_0	D_1	D_2	D_3		a	b
1	0	0	0		0	0
0	1	0	0		0	1
0	0	1	0		1	0
0	0	0	1		1	1

☑ **FUNCTION:-**

$a = D_2 + D_3$

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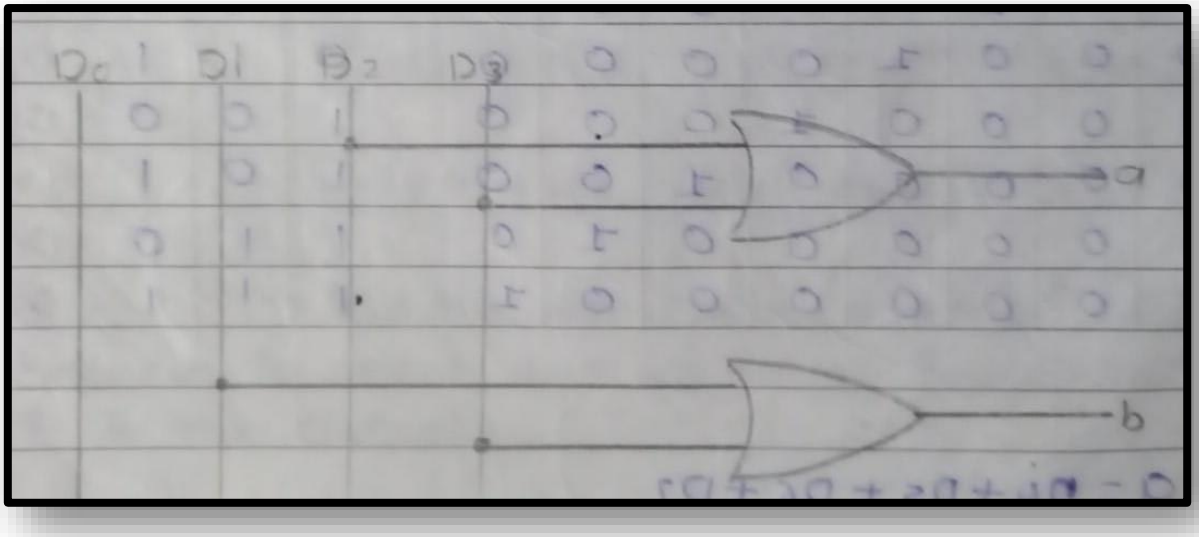
b = D_1 + D_3

Logic Circuit



☑ In the above diagram **their are 4 i**nput like **D0, D1, D2, D3** and their **are 2 output like a, b.**

☑ One Marks Questions:- ☑

Question	Answer
1. ENCODER MEANS?	OPPOSITE PROCESS OF DECODER

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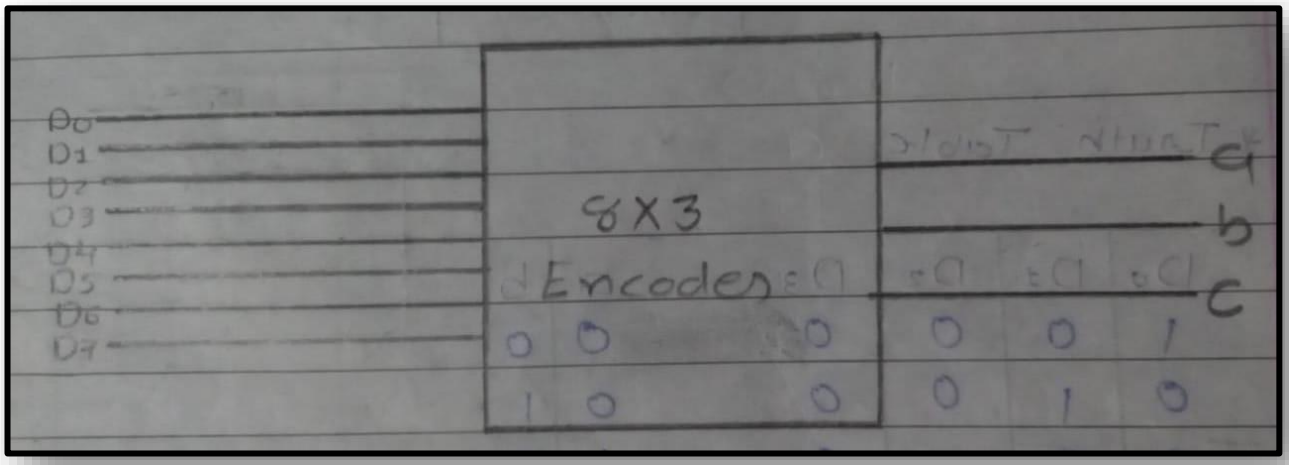
Q-5. 8 X 3 LINE ENCODER.

DETAILING:

☑ Encoder is **combination of circuit.**
☑ Encoder convert **human language into binary language.**
☑ **In 8 x 3 line** encoder has **8 inputs** like D0, D1, D2,.....D7 and their are 3 output like a, b, c.



Block Diagram

Truth Table

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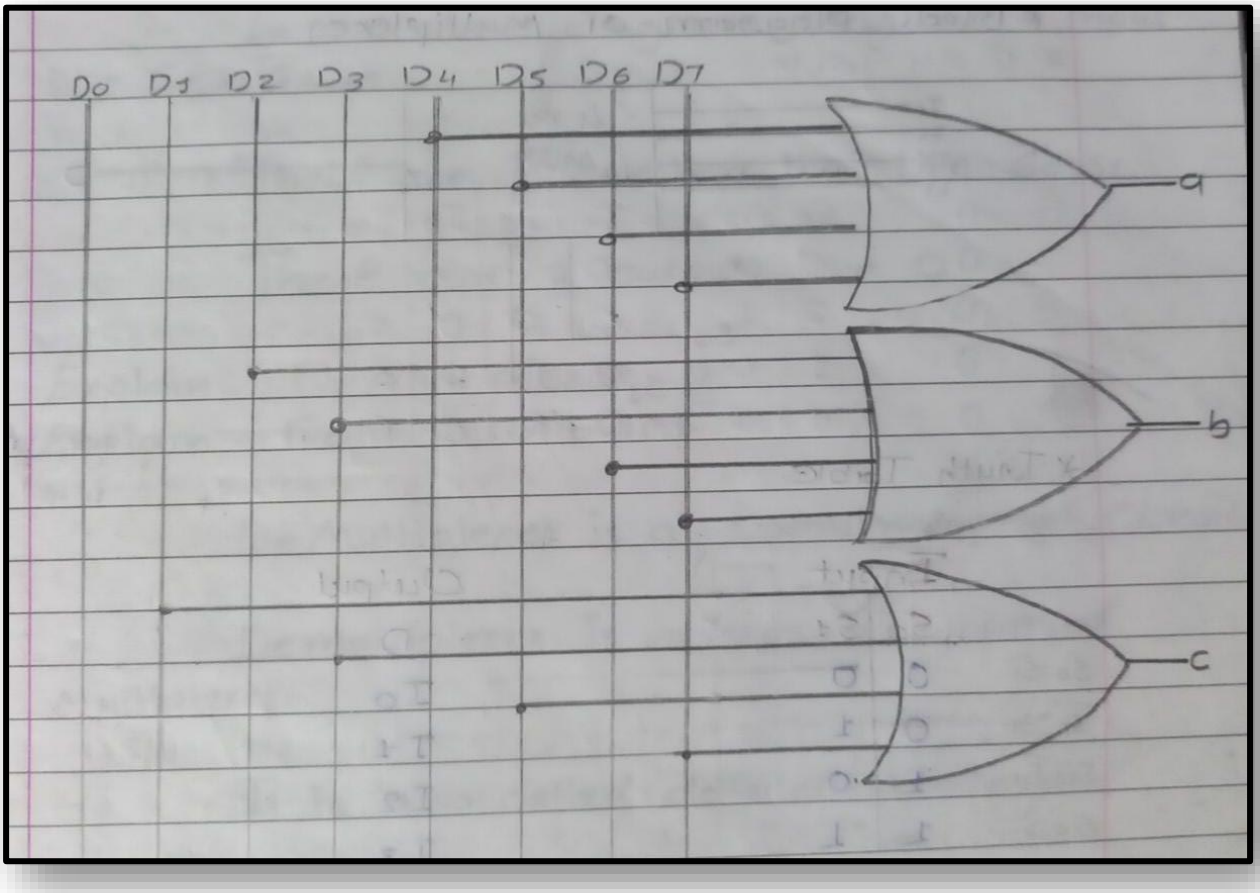
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7		a	b	c
1	0	0	0	0	0	0	0		0	0	0
0	1	0	0	0	0	0	0		0	0	1
0	0	1	0	0	0	0	0		0	1	0
0	0	0	1	0	0	0	0		0	1	1
0	0	0	0	1	0	0	0		1	0	0
0	0	0	0	0	1	0	0		1	0	1
0	0	0	0	0	0	1	0		1	1	0
0	0	0	0	0	0	0	1		1	1	1



Logic Circuit A=D4+ D5+D6+D7 B= D2+D3+D6+D7 C=D1+D3+D5+D7

☑ One Marks Questions:- ☑

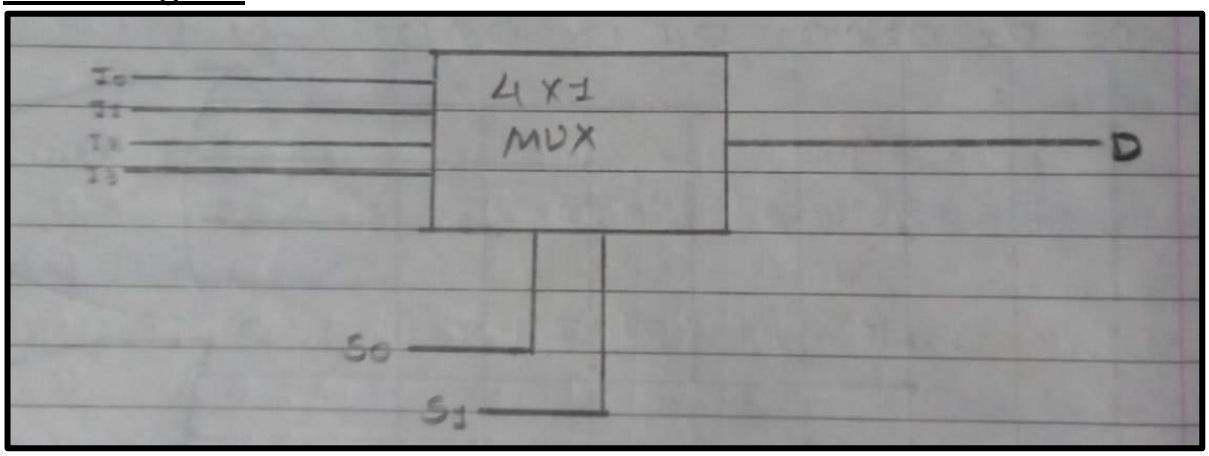
Question	Answer
1. ENCODER MEANS?	OPPOSITE PROCESS OF DECODER

Q 6 EXPLAIN MUX. OR
EXPLAIN MULTI PLXER. OR
EXPLAIN DATA SELECTOR. OR
EXPLAIN 4 X 1 LINE MULTI PLEXER.

DETAILING:

☑ Multiplexer is **combinational circuit.**
☑ It is also called **data selector.**
☑ Multiplexer **means many into one**. Because **it select one of many** input and **direct it to the output.**
☑ The selection of input is control by selection line (input)

Block Diagram



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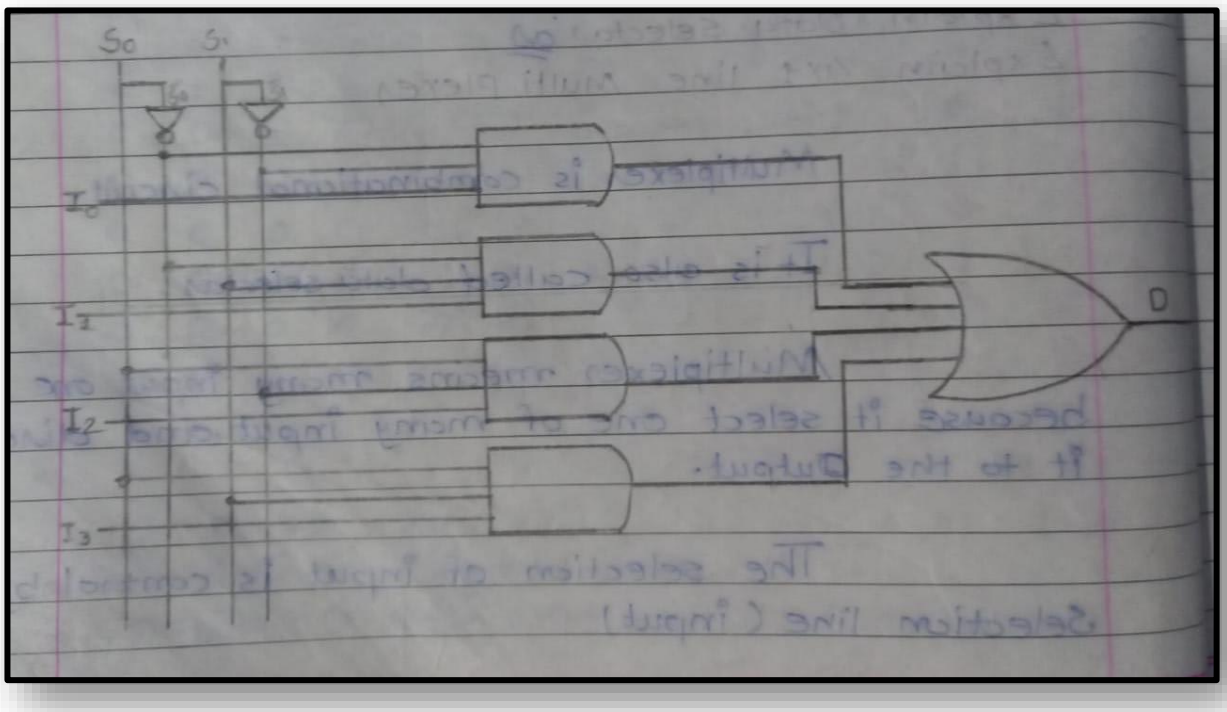
Truth Table

Input		Output
S_0	S_1	D
0	0	D
0	1	D
1	0	D
1	1	D

Logic Circuit



☑ In the above diagram their are 4 input like I0, I1, I2,3.

☑ Their are 2 selection line like S0, S1.
☑ There are 1 output like D.

☑ One Marks Questions:- ☑

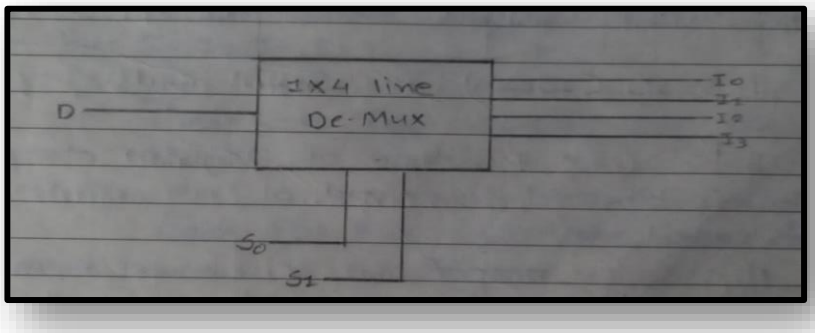
Question	Answer
1. MUX MEANS___	MULTIPLEXER
2. MUX IS ____	DATA SELECTOR

Q7 EXPLAIN DEMULTIPLEXER
EXPLAIN DATA DISTRIBUTER.

DETAILING:

☑ Demultiplexer is a **combinational circuit**
☑ Demultiplexer is **revers operation** of multiplexer
☑ It is also called **Data Distributer.**
☑ It is **transmit** the **same data** of the **different part.**
☑ De Mux **means 1** Into **many.**

Block Diagram



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Truth Table

Input
D
D
D
D
D

Input	
S_0	S_1
0	0
0	1
1	0
1	1

S_0	S_1
0	0
0	1
1	0
1	1

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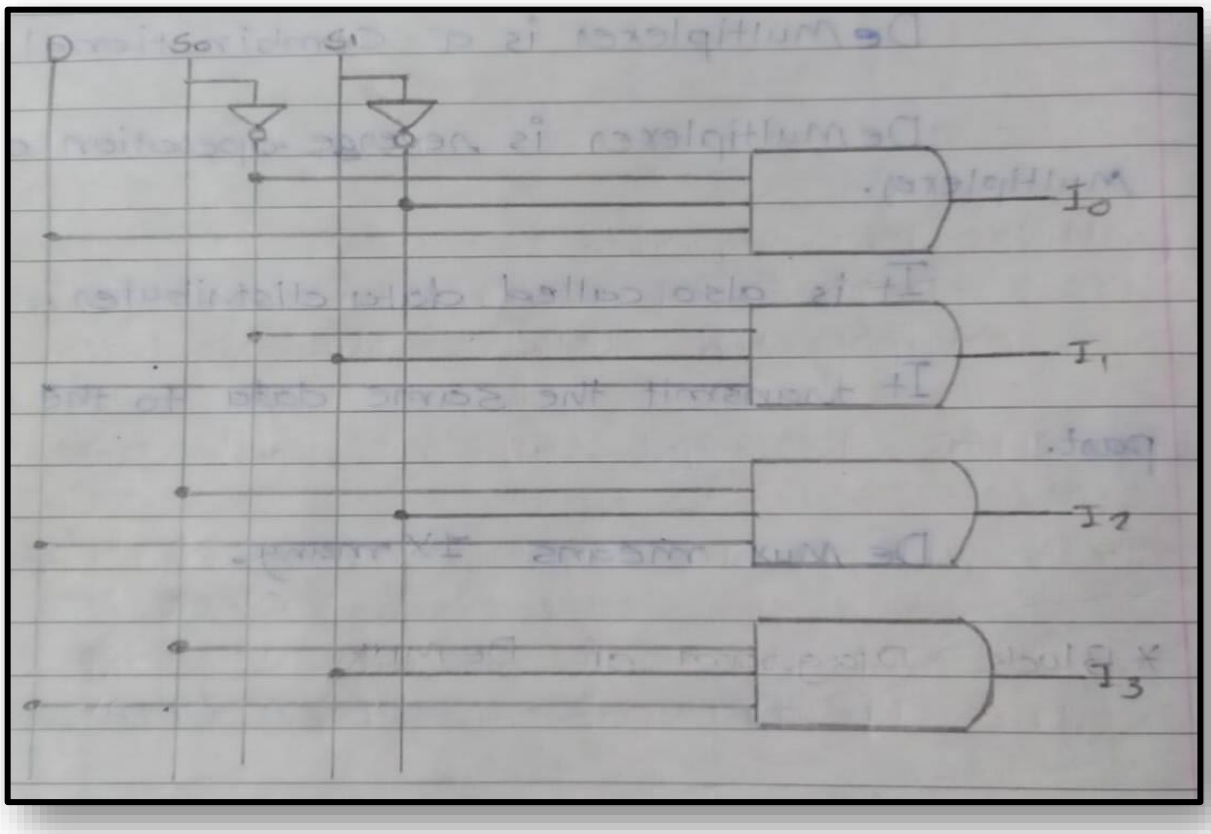
Logic Circuit



☑ One Marks Questions:- ☑

Question	Answer
1. DMUX MEANS___	DEMULTIPLEXER
2. DMUX IS ____	DATA DISTRIBUTOR

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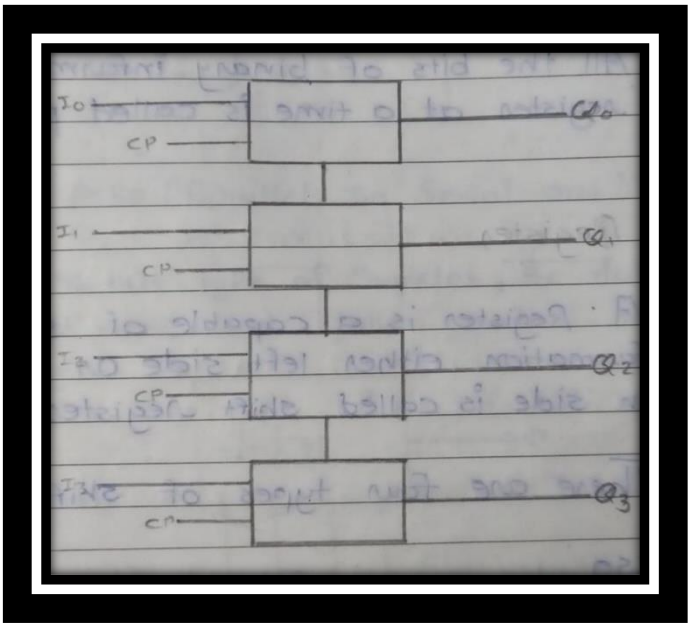
Q 8 EXPLAIN REGISTER. OR
EXPLAIN SHIFT REGISTER. OR
EXPLAIN 4 BIT BINARY REGISTER.

DETAILING:



☑ Register is **collection** of **one or more than one flip- flop**.
☑ In the above diagram there are **four input like I0, I1, I2, I3**
☑ There are **four output** like Q0, Q1, Q2, Q3.
☑ **Each flip-flop has one clock** input to control process in the register.

☑ **Types of Register**

- There are **two types of register** like **parallel register** and **shift register**

1. Parallel Register.

☑ All the bits of **binary information** are **load into register at a time** is called parallel register.

2. Shift Register.

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☑ A Register is a **capable of shifting** binary information either **left side or right** side **or in both side** is called Shift register.

☑ There are four type of shift register.

1. SISO (SERIAL IN SERIAL OUT)
2. SIPO (SERIALIN PARALLE OUT)
3. PISO (PARALLEL IN SERIAL OUT)
4. PIPO (PARALLEL IN PARALLEL OUT)

1. SISO (SERIAL IN SERIAL OUT)

☑In this type of register data is **store bit by bit** and **taken out** of the register **serially** is called SISO.

2. SIPO (SERIAL IN PARALLEL OUT)

☑ In this type of register the data is taken into the register **bit by bit** and taken out **Parallel Mode** is called SIPO.

3. PISO. (PARALLEL IN SERIAL OUT)

☑ In this type of register, the data is **entered parallel mode** and taken out of the register **serially.**

4. PIPO (PARALLEL IN PARALLEL OUT)

☑ In this type of register, the data is entered in the **parallel mode** as well as taken out to the register in **parallel Mode.**

☑ One Marks Questions:- ☑

Question	Answer
1. HOW MANY TYPES OF REGISTER?	2

2. SISO MEANS	SERIAL IN SERIAL OUT
3. SIPO	SERIAL IN PARALLEL OUT
4. PIPO	PARALLEL IN PARALLEL OUT

Q-9 EXPLAIN COUNTER.

DETAILING:

☑ Counter is nothing but a **register** that **capable of counting** the **clock input** into the **register**.
☑ Counter is also called **binary Counter**.
☑ In the counter, Mainly **J - K flip-flop is used**
☑ In the above diagram three-bit binary register has **three clock pulse** and **two input like J and K.**
☑ There are three output like **Q0, Q1, Q2**.
☑ There are two types of counter **ripple** counter and **Asynchronous** counter.
☑**Ripple counter** count **clock pulse in parallel mode** where as **Asynchronous counter count** in the **sequence.**

☑ One Marks Questions:- ☑

Question	Answer
1. COUNTER MEANS__	IT COUNT CLOSE PULSE IN THE REGISTER
2. HOW MANY TYPES OF CONTER?	2

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CHAPTER- 3 DATA REPRESENTATION

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→ Binary Addition: -

DETAILING:

```
  0     0     1     1     1
+ 0   + 1   + 0   + 1   + 1
---   ---   ---   ---   + 1
  0     1     1    10    ---
                          11
```

1+1+1+1= 10
1+1+1+1+1= 11
Note. Even =10 , Odd = 11

→ (111 + 101) perform addition.

```
  1 1 1      1 1 1 1      1 1 1
+ 1 0 1    + 1 1 1 1    + 1 0 1
-------    ---------    + 1 1 0
1 1 0 0    1 1 0 0      -------
                        1 0 1 0
```

→ Binary Multiplication

DETAILING:

```
    1 1 1
*   1 0
-------
0 0 0 0
1 1 1 0
-------
1 1 1 0
```

```
    1 1 0 1
*   1 0 1
---------
    1 1 0 1
  0 0 0 0
+ 1 1 0 1
---------
1 0 0 0 0 0 1
```

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→ Binary Division

DETAILING:

```
      1 0 1
    ---------
1 1 | 1 1 1 1
    - 1 1
    ---------
      0 0 1 1
    -     1 1
    ---------
      0 0 0 0
```

```
        1 0 0 1
      -----------
1 1 0 | 1 1 0 1 1 0
      - 1 1 0
      -----------
        0 0 0 1 1 0
      -       1 1 0
      -----------
        0 0 0 0 0 0
```

Q-1.EXPLAIN ERROR DETECTION CODE OR EXPLAIN PARITY BIT.

DETAILING:

☑ There is **1 bit** that **detected error** during transmission of data is known as **pairty bit**.
☑ Parity bit us used as **error detection code.**
☑ Parity bit can **detected present** of **error** during data transmission.
☑ Error detection is **ability** to **detected the error.**

☑ One Marks Questions:- ☑

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Question	Answer
1. PARITY BIT DETECT__	ERROR
2. PARITY MEANS	PAIR OF BIT
3. PARITY BIT IS ALSO CALLED____	ERROR DETECTION CODE.

Q 2 Explain floating point representation.

DETAILING:

☑ Floating point representation is method to **represent numerical data** in the **memory cell**.
☑ In the floating point there are **two parts** like **Mantissa and Exponent.**

1. Mantissa

☑ Mantissa part should be greater than or equal to **0.1** and **less than 1.**

Ex. 12.4566
Then M= .4566

2 Exponent

☑ It means **power** of value.
☑ It is **represented** as **"E"**

Ex. $10.10 * 10^{-3}$
Then $E = 1^{-3}$

☑ One Marks Questions:- ☑

Question	Answer

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1. **ERROR DETECTION CODE IS CORRECT ERROR??**	**NO**
2. **HOW MANY PART IN ERROR DETECTION CODE?**	**2**

CHAPTER- 4 C. P. U.
14 MARKS
22 LECTURES

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6	**REGISTER STACK**
7	**NOTATION**
8	**INTERRUPT**

Q-1 EXPLAIN CPU AND COMPONENTS OF CPU. (5- MARK)

DETAILING:

☑ The part of computer system that perform the **bulk data processing** is call **CPU.**
☑ CPU is **heart** of **digital computer**.
☑ It performs **all** the **function** and **variety of code.**
☑ CPU are **made up** of **three major Part.**

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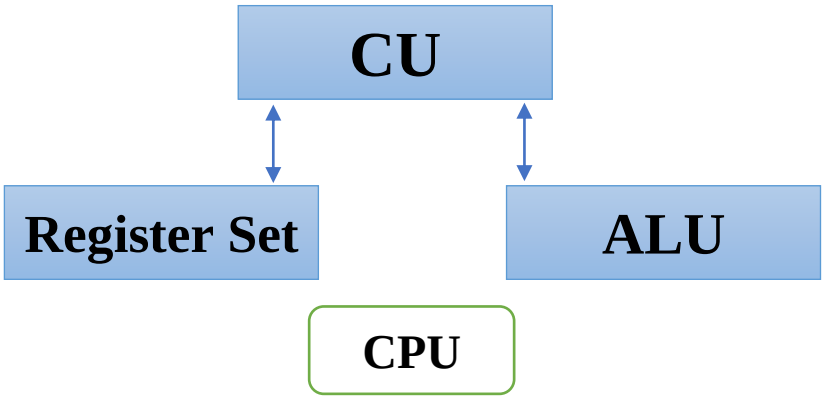
Block Diagram of CPU



*

☑ There are **three** major **components** of CPU like **control Unit, Register set** and **ALU**.

1) Control Unit

☑ Control Unit **monitor** the **transfer the data** of information to the computer device.
☑ Control unit **control** all the **operation and code.**
☑ Control unit **monitor** all the **input output.**
☑ Control unit **instruct** the **ALU** which **operation** to be **perform.**

2) ALU

☑ The **ALU** of computer is **place** where **actual data process.**
☑ It is **multiprocessing digital unit**.
☑ It can **perform** set of **basic arithmetic** and **logical operation.**
☑ This **part** of **microprocess** is **responsible** for **perform addition, Subtraction, Multiplication, and Division.**
☑ It performs **required micro operation.**

3) Register Set:-

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☑ Register set **store Binary** Information **into the register.**

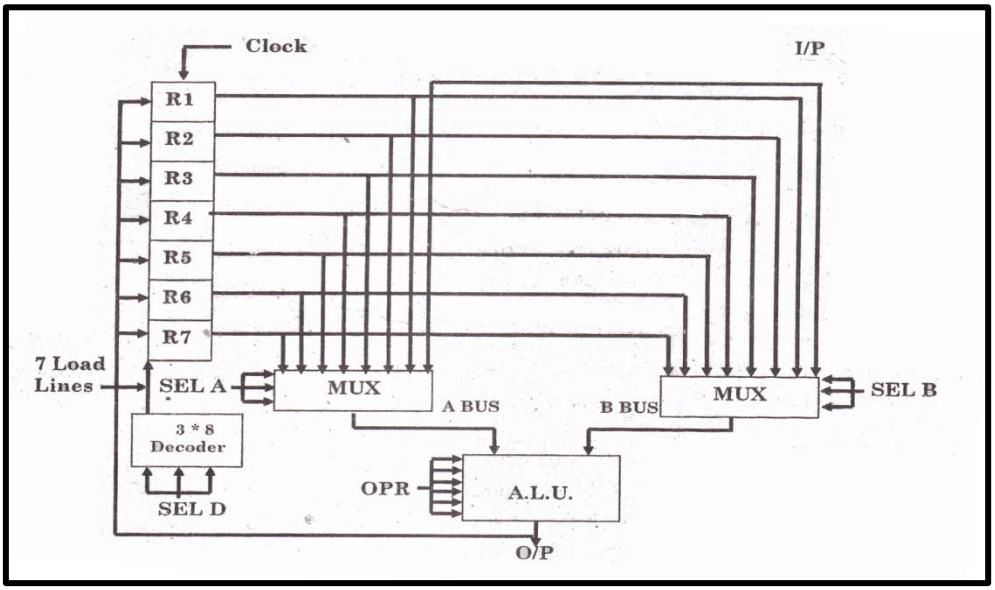
☑ One Marks Questions:- ☑

Question	Answer
1. CPU IS ___ OF COMPUTER?	HEART
2. CPU MADE UP WITH ___ MAIN PART	3
3. ALU MEANS____	ARITHMETIC AND LOGIC UNIT

Q.2 Explain General Register Organizer. (5 Mark) (MIMP)

DETAILING:

☑ There are **large number** of **registers** to be include **inside the CPU.**
☑ This register is **called processor register.**
☑ This processor register are **inter connected** with each other **inside the CPU.**



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☑ In the above diagram……..
☑ There are **7 processor** register like **R1, R2, R3,…….R7** This register are used to **store binary information.**
☑ There are **2 multiplexer** like **MUX A** and **MUX B**.
☑ There are **two control words**. **Sel A** and **Sel B.**
☑ There is **arithmetic and Logical unit** to be used to perform pacific **micro operation.**
☑ There is 1 Control word **like opr.**
☑ Control word **opr** is used to select which **micro operation** to be **performed by ALU**.
☑There is **1 decoder** to be used to **select destination** register to **store generated output**.
☑ Control word **sel D control** the **decoder.**
☑ There is **1** external **Input line**. It may be connected with **another memory device**.
☑ There is **1 output** line is used to **store result** into **either processor** register **or another memory device.**

☑ One Marks Questions:- ☑

Question	Answer
1. PROCESSOR REGISTER IS INTERCONNECTED WITH EACH OTHER?	YES
2. HOW MANY CONTRO WORDS ARE IN REGISTER	4

Q- 3 EXPLAIN CONTROL WORD. (3- MARK)

DETAILING:

☑ There are **4 control word** in the general **register** organization.
☑ Working of each control words describe as per the following.

1. **Sel A**

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☑ Sel A has **3** Control input **signals** to the control operation on the **MUX A**.

2. SEL B

☑ Sel B has **3** Control **input** signals to the control operation on the **MUX B**.

3. Sel D

☑ Sel D has **3** Control input signals to the **control** operation on the (3 X 8) **decoder.**

4. OPR.

☑ Opr has **5 control** input signals to control operation Alu to describe which **micro operation** to be performed by **ALU.**

☑ Using **sel A** and **sel B**, we can **select** source **register** or source **input for the ALU.**

☑ **Sel D** is used to select **destination** register to **store output**.

Q-4 EXPLAIN A REGISTER. OR
EXPLAIN AR REGISTER OR
EXPLAIN AC REGISTER OR
EXPLAIN ACCUMULATOR REGISTER.

DETAILING:

☑ **Some process** unit has **1 separate** register from all other **it call accumulator register**.
☑This Register is also **call A** register, **AC register**, and **AR register**.
☑ The **name** of this **register** is **divided** from the **arithmetic addition process.**
☑ The **A register** is **multipurpose register** capable of performing not only add microoperation but it can **perform** many **other operation.**

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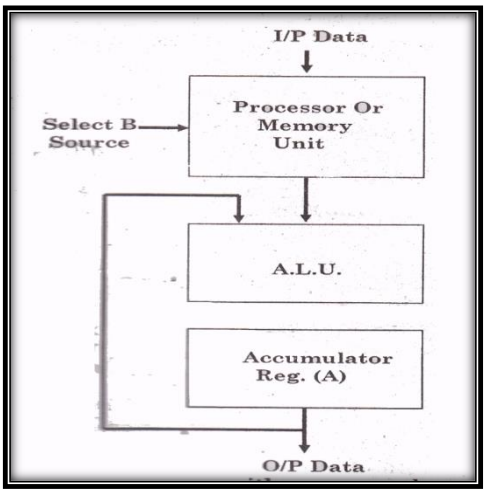
Block Diagram.



☑ In the above diagram **ALU passes** the data to the **A register**, A register can **check** the data **if data** is **correct** than **it will return** to the **output device.** If data is **not correct**, A register can **return** it to the **ALU.**

☑ One Marks Questions:- ☑

Question	Answer
1. A means ____	Accumulator register

Q-5 EXPLAIN STACK ORGANIZATION.

DETAILING:

☑ Stack is **storage unit** that store binary information in **LIFO manner.**
☑ In the Stack organization there is **1 register** is used to **store address of stack** This register is called **Stack pointer**.
☑ Stack pointer consist **address** of binary information which is **store top of stack.**
☑ There are **two** major operation of stack organization like **PUSH and POP.**

1) Push Operation

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☑ Push operation is **add** new **binary information** into the stack is called Push operation.
☑ This new binary information always **place** at the **top of stack.**

2) Pop Operation

☑The operation of **delete** binary information from the top of stack is **called POP** operation.
☑The POP operation **always** remove binary information from the **top of stack.**

- **Type of Stack: -**

1. Register Stack
2. Memory Stack

1) Register stack: -

Block of diagram

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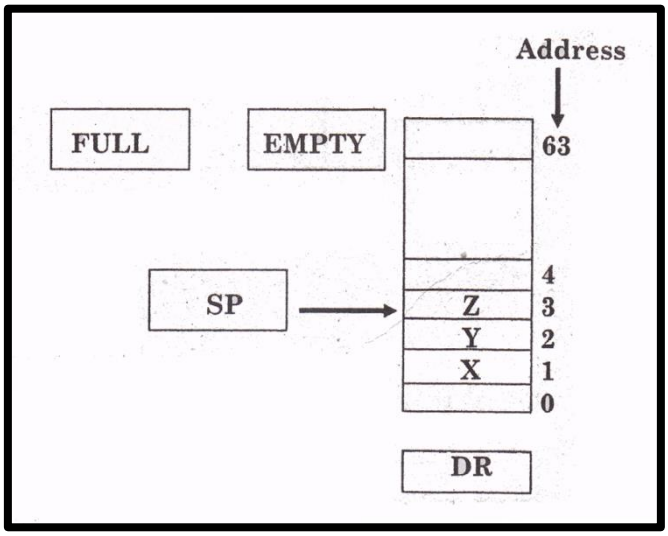


☑ The following diagram **describe** register stack which can store **64 words.**
☑ In the above diagram there are **four register.**

1. **Data Registers: -**

☑ It can store information when we perform either **push** operation or **pop operation**, binary information is **store into data register.**

2. **Stack Pointer Register** –

☑ In the stack organization there is 1 register is used to **store address of sack** is called stack pointer register.

3. **Full Register: -**

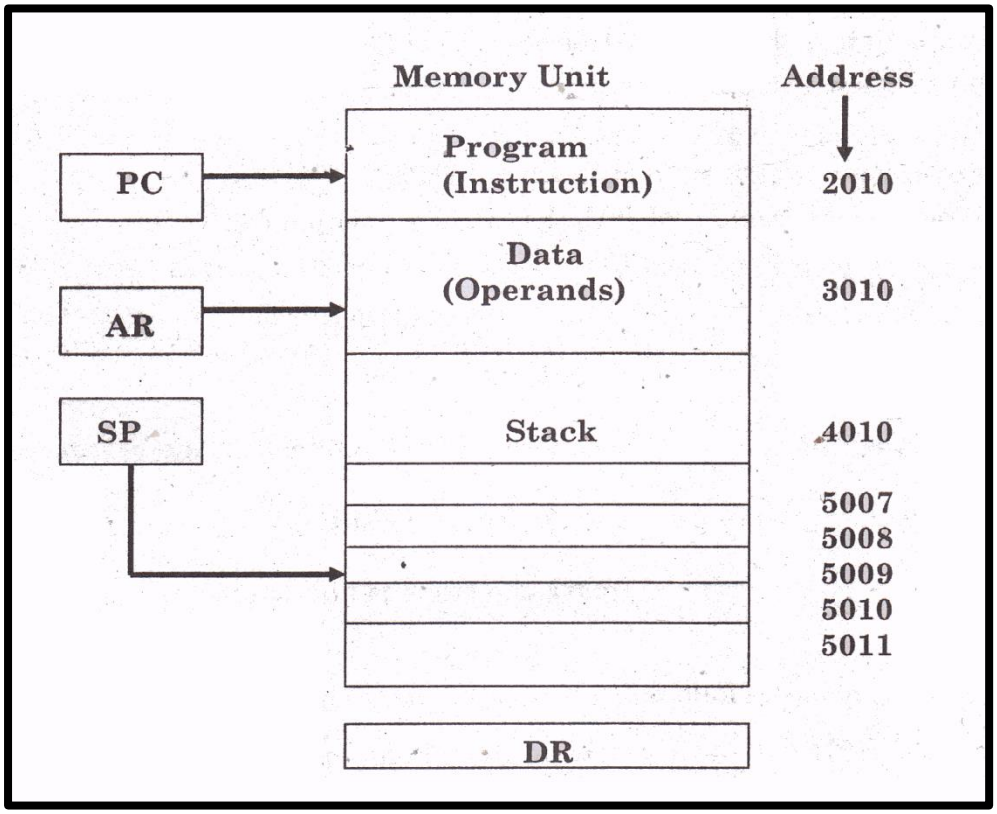
☑ Full register can **store 1** bit information.
☑ Full register indicates their stack is **full or not**.

4. **Empty Register:-**

☑ It can store **1 bit** information.
☑ Empty register indicate that stack is **Empty or Not**.

2) Memory Stack

☑ Register **stack is separate unit**. It available **inside** the **CPU** and **works as processor**.
☑ Memory stack is a **part of main memory.**
☑ In a above diagram there are three segment like programe segment, data segment and stack segment.



1) Program segment

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☑ It is used to **store instructions.**
☑ There is **1 register** available with program **segment is called program counter**.
☑ Program counter is used to store the **address** of **next instruction**

2) Data Segment

☑ It is use to **store operand.**
☑ There is **1 register** available with data segment is called **Address Register**.
☑ Address register is used to **store** address of **operand.**

3) Stack segment

☑ Stack segment is used to **store binary** information in **LIFO manner**.
☑ The stack pointer register is used to **store memory address** of binary **information**
☑ Program counter, address register and stack point are **connected** with **main memory using common bus**.

☑ One Marks Questions:- ☑

Question	Answer
1. How many stack is available?	2
2. Stack is store data in___ manner?	Lifo

Q- 6 EXPLAIN RPN
OR
EXPLAIN REVERSE POLISH NOTATION
OR
EXPLAIN PUBLISH NOTATION.

DETAILING:

☑ A stack organization is very powerful tool to **calculate**, **arithmetic operation**.
☑ The comma arithmetic expression is **written into infix notation.** That means each **operator written between operand value** for example **a + b** is **infix notation.**
☑ To calculate any arithmetic operation into stack organization it must be convert **into polish notation.**
☑ There are **three** type of notation like **infix, postfix, and prefix.**

1. Postfix notation

☑ It means each operator **written after operand value**
☑ **Ex. ab+**

2. Prefix notation

☑ It means each operator **written before the operand value**
☑ **Ex. +ab**

3. Infix notation

☑ It means each operator written **between operand** value.
☑ **Ex. a + b**

Q-7 EXPLAIN INTERRUPT.

DETAILING:

☑ The concept of program **interrupt** is used to **handle variety of problem** that **arrive out of** normal **program sequence**.
☑ The interrupt facility is **useful** in **multiprogramming** environment.

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☑ When **two** or more **program** is reside in the memory at the same time, the function of interrupt facility is **take care of data transfer** of one or more program. While another program is executed.

☑ **Type of interrupted**

☑ There are **three** type of interrupt like

1. Internal
2. External
3. Software

1) External Interrupt

☑ The external interrupt **use** by **external event.**
☑ That come from **I/P- O/P device** request transfer of data, input- output device finish transfer of data or **power failure.**

2) Internal interrupt

☑ It is also called **traps**.
☑ Internal interrupt are **come** from **internal part** like **register overflow, stack overflow and invalid operation code.**
☑ Like external interrupt this input also used signal that occur in the hardware of the CPU.

3) Software Interrupt

☑ It is **special cell**.
☑ This instruction provide switch from CPU user mode to the supervisor mode.
☑ This interrupt comes from **any type of software**.

☑ One Marks Questions:- ☑

Question	Answer

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1. When interrupt come?	When two or more program are reside into computer
2. Internal interrupt is also called ____	Traps

CH-5 INPUT- OUTPUT ORGANIZATION
14 MARKS
20 LECTURES

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Q-1 EXPLAIN MEMORY BUS

DETAILING:

☑ Input- Output organization **provide environment** for **transfer information** between **internal storage** and **external input- Output**.

Block Diagram:

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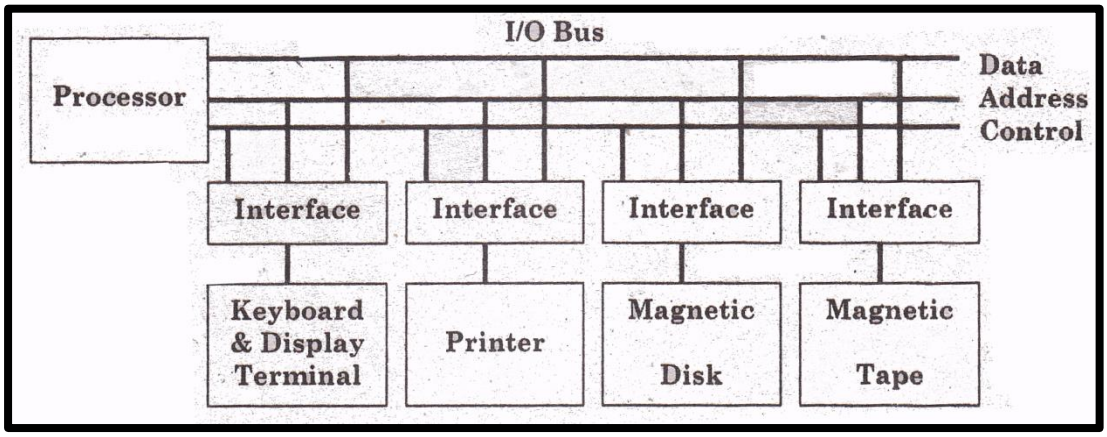
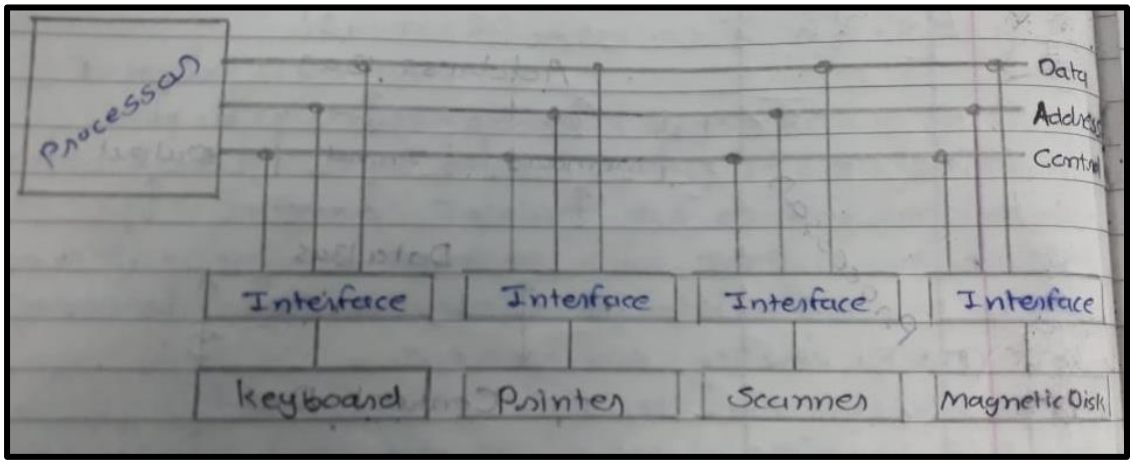


☑ In the memory bus there are three **layers** of bus available like **Address bus, Data bus and control bus.**
☑ Data bus can **collect** all the **data from input device** and **memory device**.
☑ **Data bus** can **give data** to the **address bus**.
☑ Address bus can **transfer information** about **memory location** from **one part** of computer to **another part of computer**.
☑ Address bus also **transfer data** to **the processor.**
☑ Processor can perform **process** of the data and **return to the data bus.**
☑ Data bus can **transmit the data** to the **address bus**.
☑ Control bus control all the processes of memory bus.

Q-2 EXPLAIN INPUT- OUTPUT BUS.

DETAILING:

☑ **Communication link** between **process** and **Input- Output device** is show **in diagram.**
☑ The **input/ Output** bus consists of **data** line, **address** line and **control line.**
☑ Each device has **associated** with **its interface**.
☑ Each **interface decodes** the **address** and **control receive** from the **input/ Output Bus.**
☑ Interface **give data** to the **data bus**. **Data bus can transmit data** to the **address bus** and address bus **transmit data** to the **processor** or **interface.**
☑ Address bus is also called **address line.**



☑ One Marks Questions:- ☑

Question	Answer
1. Io means _____	Input and output
2. Iop means	Input output processor

Q-3 EXPLAIN INPUT/ OUTPUT PROCESS.

DETAILING:

☑There is **separate process** communication **with all the I/O device** and control **them is known as IOP**.
☑ In some **digital system** there are **more then one IOP** .
☑ **IOP** keep **watching data** during **transmission between I/O device.**
☑ If any micro computer system has I/O all the **signal control** by the **IOP.**
☑ That means **I/O fetch** and **execute all the I/O instead of CPU.**

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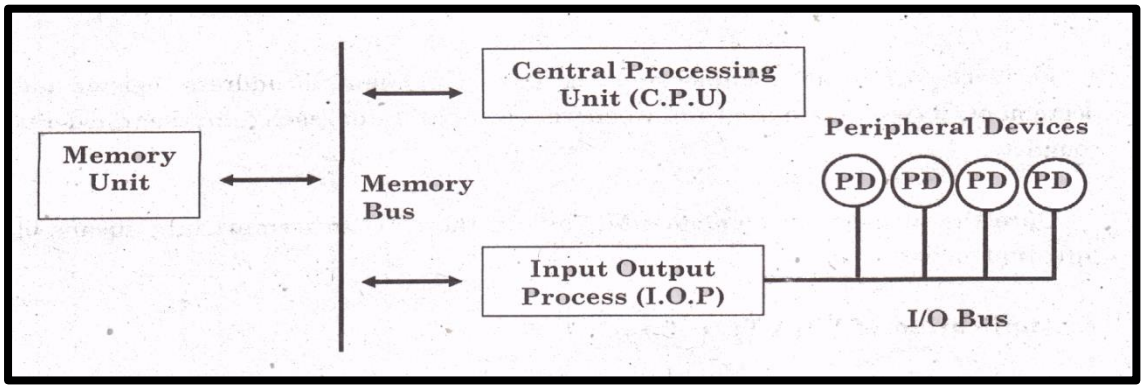

☑ In the above diagram **CPU is master** processor and **I/OP is slave**[Second] **processor.**
☑ IOP provide **interface** to **communicate** in between **I/O device** and **memory unit** using memory bus.
☑ There are some **control signal** is used to **communication** in between **IOP & CPU.**

☑ One Marks Questions:- ☑

Question	Answer
1. pdp means _____	Peripheral device
2. Iop means	Input output processor

Q- 4 EXPLAIN I/O INTERFACE.

DETAILING:

☑ **I/O** device **connected** to the **CPU** by **using special communication link**, this link are **known as I/O interface.**

Q-5 EXPLAIN BUS.

DETAILING:

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☑ A collection of **hardwire** which are **arrange** in parallel form using **transfer** the **binary** information in between **computer device** is **called Bus.**
☑ Using Bus we can **transmit binary information** like data, address and many other information.
☑ Binary information **travel by the bus** in the form of **pulses** either **0 or 1.**

◆ Characteristics of Bus: -

1) **Size of bus**

☑ It specify that how many bit to be carry by the bus at a time.

2) **Sped of bus.**

☑ It is specify that number of bit travel in between computer device at a time.

3) **Capacity of bus**

☑ Capacity of bus= size of bus x speed of bus

◆ Type of bus:-

1) **Data bus**

☑ Data bus can **transmit data** from **one** part to **another part** of computer.

2) **Address bus**

☑ Address bus **transmit information** to the one part of computer to another part of computer.

3) **Instruction bus**

☑ It can transmit **control signal** from one part to another part of computer.

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4) System Bus

☑ It is a **special bus**. It is used to **connect path** between CPU and main memory.

5) Input/ Output Bus

☑ It is useful to **connect** processor with Input. Output device.

6) Internal Bus

☑ Internal bus **available inside the processor.**

7) External bus

☑ External bus is available to the **Outside of the processor.**

☑ One Marks Questions:- ☑

Question	Answer
1. WHAT IS BUS?	Bus travel data from one part to other part in computer
2. How many bus are available?	7
3. Internal bus available in ____	Inside the cpu

Q-6 WHAT IS DMA? WHAT IS DMA TRANSFER.

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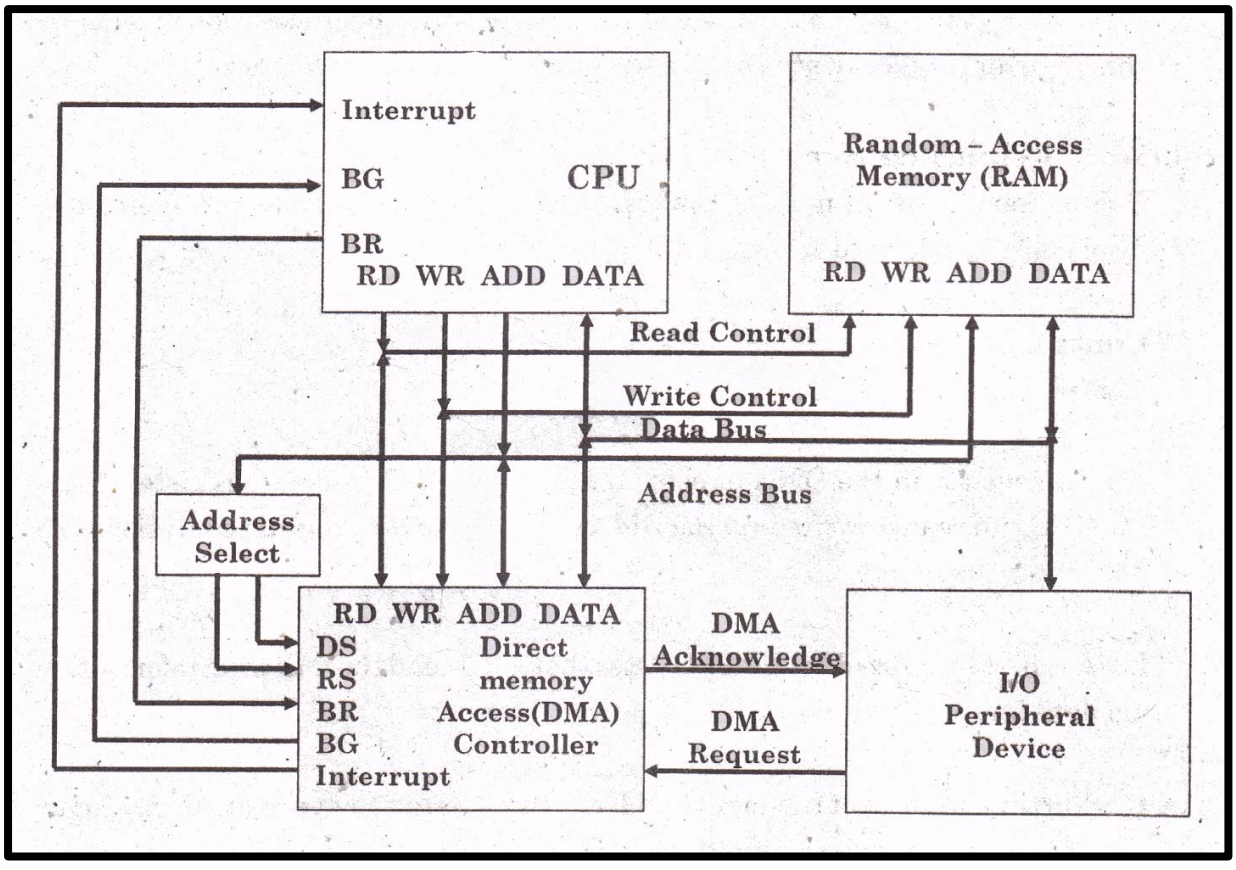
☑ Generally, CPU **control data transmission** process **between computer peripheral device.**
☑ But some time **data transmission process** and **data transmission is done** by computer device.
☑ To control data transmission process in between computer device, **special device is use.** This **device is known as DMA controller** and this data transmission technique is known as DMA[Direct Memory Access



- **DMA Transfer.**

☑ The block diagram of DMA transfer is following figure
☑ The **CPU communication** with DMA by using **data bus** and **address bus**
☑ DMA has its own address which **active DS and RS line.**

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☑ CPU initialize the **DMA throughout** the data bus and once it receives the start control combined. It can start the transfer between peripheral device the and the memory.
☑ When the device send **DMA request the DMA controller** activate BK Line which informant the CPU to realize bus.
☑ CPU respond with its **BG Line** informant to the DMA that is bus are **disable.**
☑ The **DMA than put** the current value of its address register into the address bus initialize the RD or WK signal and send acknowledgement to the peripheral devices.
☑ When **Ba= 0,** the Rd and WR input line **allow** the CPU to communicate with **DMA.**
☑ Then Ba is the **RD & WR the output** line from the DMA controller to the RAM.
☑ From each word that is **transfer**, the DMA implement its address register and decrement its word count register, when word count register reach 0 the transfer is complete.
☑ Once the transfer is completed the **DMA info** the CPU to transmit by means of **interrupt signal.**

- **Application of DMA transfer**

☑ It is may be useful in many applications between **magnetic disk & memory.**
☑ It is also useful for **update display** in interactive terminate.
☑ The contain of transfer to the screen periodically, by means of **DMA transfer.**

☑ One Marks Questions:- ☑

Question	Answer
4. DMA MEANS	DIRECT MEMORY ACCESS
5. DMA IS ___	CONTROLLER
6. DMA IS CONTROL ____	SPEED OF OTHER DATA TRANSMISSION

Q- 7 EXPLAIN WORKING OF DMA. [05 MARK]

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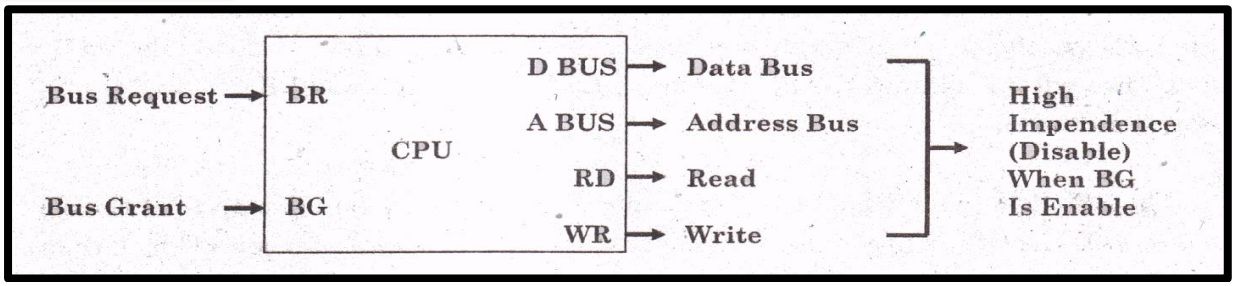
DETAILING:



☑ Drawing DMA **data transmission CPU** use some control signal.
☑ This control signal is use listed as per the following.

1) Bus Request.

☑ **BR** control signal is **generated by DMA** and pass the **CPU**.

2) Bus Grand(BG)

☑ This signal is generated by **CPU** and **pass to the DMA controller.**
☑ Using **BR signal DMA controller** pass request to the **CPU to relies a**ll the memory bus as well as read write line.
☑ When **BR** signal become enable, **CPU stop the current process.**
☑ After this process CPU enabled **BG control signal.**
☑This **BG signal info** to the DMA controller to memory bus are disable.
☑ After this process **DMA controller** control all the memory bus as well as control line.
☑ Now, using DMA controller the **transmission control** done between computer device without intervention of CPU.
☑ After completion of **data transmission process** bus request line become disable there for CPU disable there for CPU disable BG control signal.
☑ After that again data transmission process **done by the CPU.**

☑ One Marks Questions:- ☑

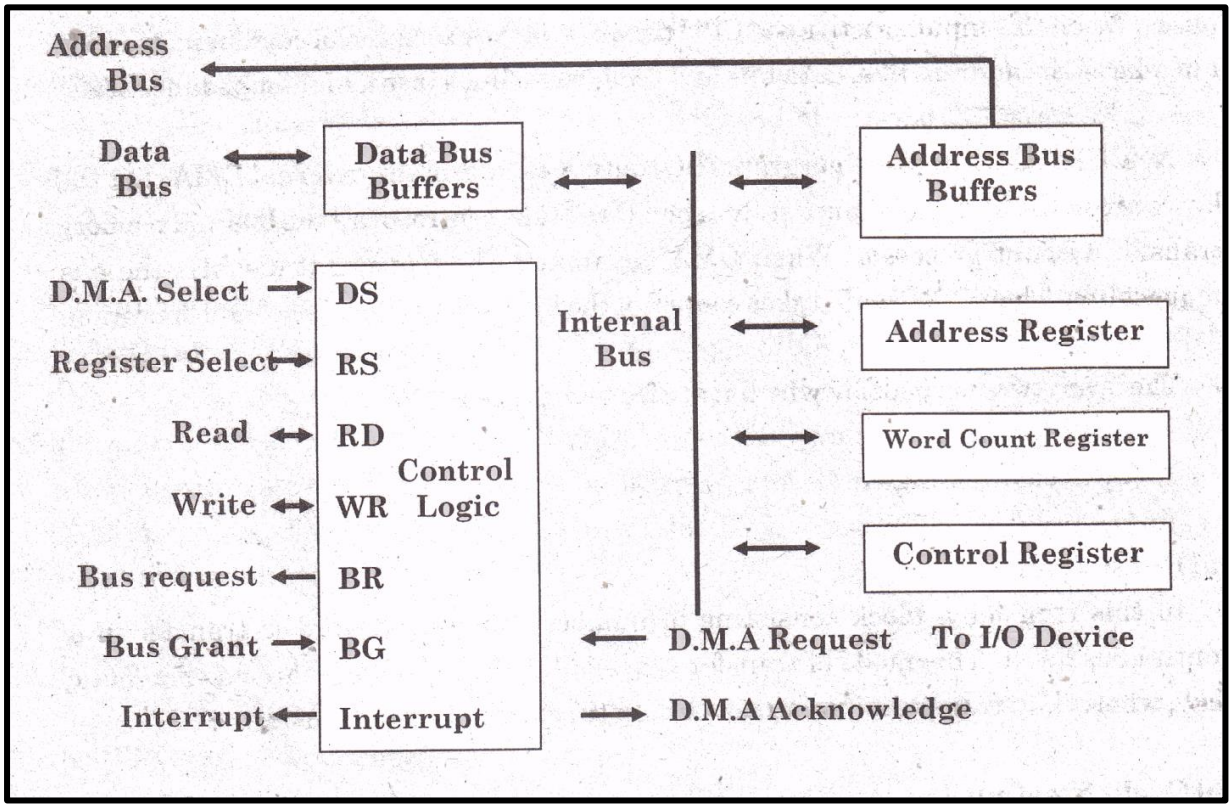
Question	Answer
7. BG MEANS ___	BUS GRANT

8. BR MEANS	BUS REQUEST
9. CPU MEANS__	CENTRAL PROCESSING UNIT

Q- 8 EXPLAIN DMA CONTROLLER [05- MARK]

DETAILING:

☑ There is one **special circuit** use to communication between **DMA controller and CPU** known as **interface circuit.**



☑ In the above diagram there are three register.

1) Address Register

☑ Address register **contain address of specific location** inside the memory device.

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☑ It is used common **address bus** to direct communication with device.

2) Word count Register

☑ This register **specifies that how many numbers of word to be transmitted** from one device to another device.

3) Control Register

☑ Control register specify **mode of transfer** during data transmission while DMA technique is used.
☑ When **DMA controller** communicate with external device, DMA request and **DMA acknowledgement are used.**
☑ This signal are **manage data** transmission during DMA technique is used to transmit data.
☑ DMA controller **communicate with CPU** by using common bus as well as some control signal
☑ There is one **interrupt to be generated** by the DMA controller and pass to the CPU.
☑ Using this interrupt **DMA controller** information to CPU to **terminate current process.**

☑ One Marks Questions:- ☑

Question	Answer
1. AR MEANS____	ADDRESS REGISTER
2 WORD COUNTER REGISTER MEANS___	IT COUNT WORD PASS INTO REGISTER

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